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STUDY OF THE PHYSICS OF INSULATING FILMS AS RELATED TO THE RELIABILITY OF METAL-OXIDE-SEMICONDUCTOR (MOS) DEVICES

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June 1, 1981 - November 30, 1981

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This report covers work on enhanced electron injection into SiO_2, studies of limitations on the number of useful write/erase cycles for EAROS devices due to electron trapping in SiO_2, the physics and design of EAROS devices using Si-rich SiO_2 charge injectors, and the capture and release of electrons on Na^+-related sites in SiO_2. An automatic system is described for making write/erase cycling measurements of EAROS devices.

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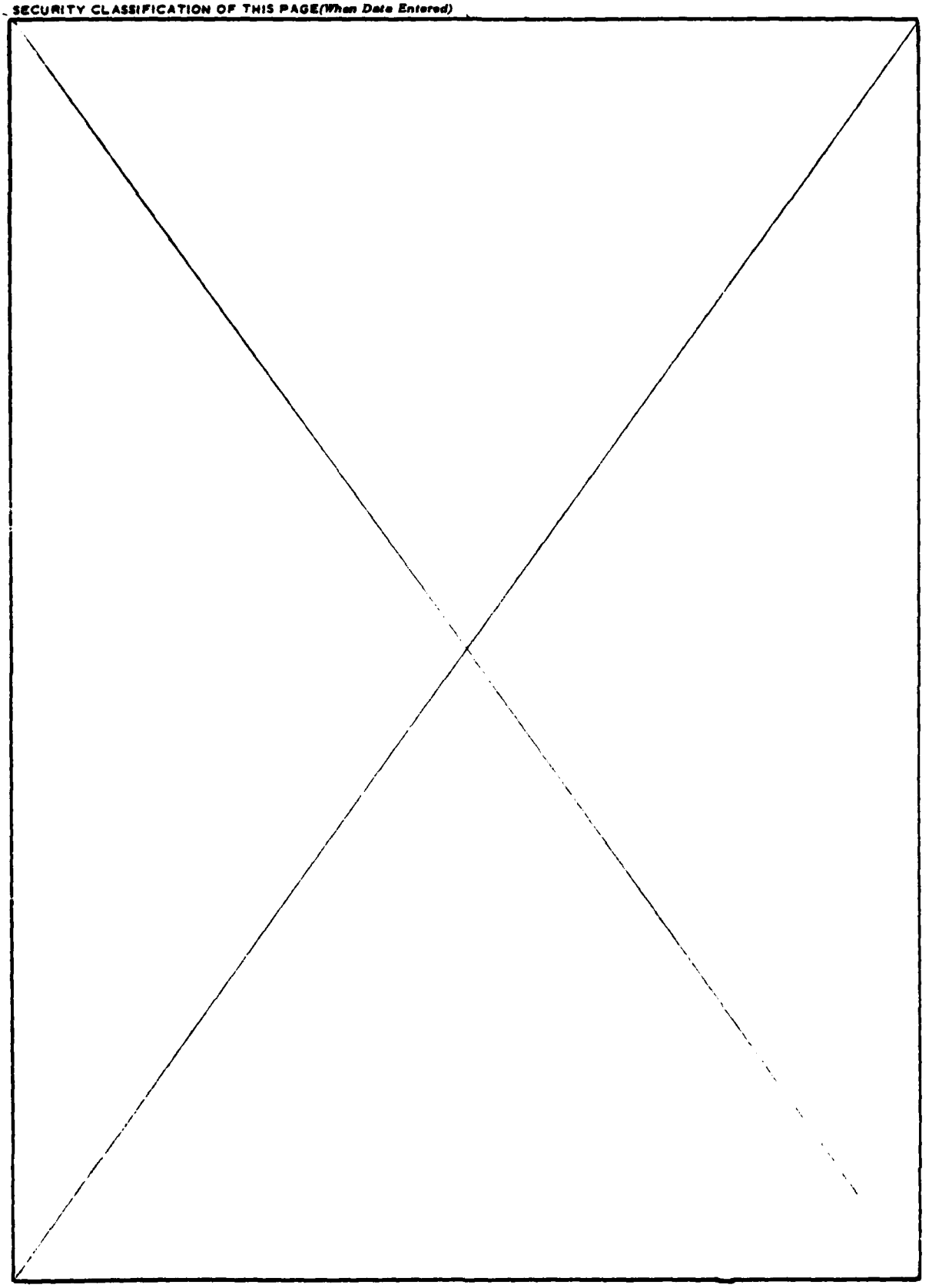

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INTRODUCTION

The work during this period continues to emphasize the use of Si-rich SiO_2 layers in charge injection structures for application to EAROM devices. The results of the work done to date continue to emphasize the utility of these structures and certainly emphasize the need for continued work in this field.

Previous papers have suggested that the mechanism for current enhancement resulting from the Si-rich SiO_2 is due to the increased local field, resulting from the presence of conducting particles in an insulator, at the conductor to insulator interface. Previous work has used Si precipitates as the particles. If this explanation is correct, it would be expected to occur if metal particles are used instead of the Si precipitates. The paper by Falcony, DiMaria and Guarnieri shows that this is indeed the case using Al, Ni and Mo-SiO_2 cermets instead of Si-rich SiO_2.

It has been recognized that the number of useful write/erase cycles in floating gate EAROMs is controlled by electron charge trapping in the intervening SiO_2 layer. As a result it would be expected that treatments to reduce the electron trapping should increase the number of useful write/erase cycles. The paper enclosed by Falcony, DiMaria, Dong and DeMeyer shows that this is the case where the specific treatment used is annealing the stack at 1000°C in N_2. A general review paper by DiMaria is included discussing the physics and engineering of EAROM devices.

It has been recognized for some time that the radiation present in a Reactive Ion Etching (RIE) Apparatus can generate neutral electron traps in SiO_2. The paper by Ephrath, DiMaria and Pesavento discusses the dependence of the damage created on the reactor parameters. Results are also shown indicating that aluminum or n^+ polysilicon gate materials are effective in shielding the oxide from the radiation that would cause this damage.

The paper by DiMaria on "Capture and Release of Electrons on Na^+-Related Trapping Sites in the SiO_2 layer of MOS Structures at Temperatures Between 77°K and 296°K" has brought together many interesting observations concerning the electron trapping behavior of Na^+ in SiO_2. This work shows that the behavior observed is completely different for low Na^+ areal concentrations ($\leq 3.7 \times 10^{12}$ Na/cm^2) than for higher concentrations. One model for the low concentration regime suggests that electrons go into shallow excited states first (at temperatures below 158°K) and then are either thermally excited back into the conduction band of the SiO_2 or sink to much deeper states that are stable up to room tempera-

ture. The results for higher concentrations ($> 3.7 \times 10^{12}$ Na/cm^2) are much more complex and are described in the paper. A discussion is also presented comparing the results of this work with studies of other workers concerning the effects of Na^+ on the behavior of inversion layers. Considerable work remains to be done to correlate the results of these various investigations.

A report by Pesavento, Lai and Calise is included that describes the design of an automatic apparatus for EAROM cycling studies.

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Enhanced Electron Injection Into SiO_2 Layers Using Granular Metal Films*

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ABSTRACT

The enhancement of electron injection into silicon dioxide layers using a metal - granular metal film - SiO_2 - silicon structure is reported for Al, Ni and Mo-SiO_2 cermets. This enhancement was found to be stronger for higher metal to oxide ratio. The I-V characteristic curves for these structures follow the Fowler-Nordheim tunneling mechanism behavior, indicating that the dominant effect is an enhancement of the electric field near the granular film - SiO_2 interface.

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Electron injection into wide band gap insulators such as silicon dioxide usually requires a large energy transfer to the free carriers in the contacts to overcome the large interfacial energy barriers formed by the contact - insulator interface.[1] Several techniques are used to achieve this purpose at low to moderate electric fields of which the most commonly used are internal photoemission[2] and avalanche injection.[3] At large electric fields ($\approx 10^7$ V/cm), carrier injection into the insulating layer from the contacts is via tunneling.[4] The injection mechanism involved is Fowler-Nordheim tunneling or direct tunneling in the case of very thin insulating layers (< 50 Å). However, the incidence of destructive breakdown is large and generally associated with localized asperities and/or impurities at the electrode interface with the insulator.

Recently the localized enhancement of the electrical field by means of a rough poly-Si interface[5,6] or a Si-rich layer in between the electrode and wide band gap insulator[7] has been used to reduce the average applied electric field required for charge injection into SiO_2 layers. The enhancement of the electric field comes from sharp asperities at the poly-crystalline Si/SiO_2 interface for the first case and from the irregular shape of Si islands, at or near the Si-rich SiO_2/SiO_2 interface for the second case. The advantage of being able to inject charge into SiO_2 layers at lower electrical fields without destructive breakdown is of particular utility in applications that require charge transfer across an insulating film as in the case of electrically-alterable read-only-memories (EAROMs).[7] In this paper, a similar field enhancement when a metal - SiO_2 cermet[8] is deposited between the electrode and the SiO_2 layer in a metal-oxide-semiconductor (MOS) structure will be described. This enhancement is found to be dependent on the metal to SiO_2 ratio in the cermet. The results for Al, Ni, and Mo cermets will be reported.

The samples were MOS capacitors with a thin (~ 200 Å) granular metal film in between the metal contact and the silicon dioxide layer. The oxide layer was thermally grown on <100> p-Si substrates at 1000°C to a thickness of 500 Å or 830 Å. A dual source

e-beam evaporation system was used to deposit the cermet and metal gate electrode formed from the same metal as used in the cermet. It should be mentioned that the reproducibility of results obtained using this sample preparation method was poor from run to run. After metallization, all samples were annealed in forming gas (90% N_2 - 10% H_2 at 400°C for 20 min.) to reduce the Si-SiO_2 surface state density and remove any trapped holes in the SiO_2 near the Si-SiO_2 interface that were introduced by the scattered radiation from the e-beam deposition process.[1] Na^+ levels in the samples were checked using flat-band voltage shifts from capacitance-voltage measurements after temperature-bias stressing and were found to be less than 10^{11} *ions/cm*^{2}. The characteristic behavior of the current as a function of applied gate voltage in these devices was measured using a ramped voltage (0.5 V/sec) applied to the metal gate electrode. A Keithley log-picoammeter No. 26000 was used to measure the current.

The behavior of the current-voltage characteristics as a function of the metal content in the cermets is illustrated in Figs. 1 to 3 where the characteristic ramp I-V curves are shown for different metal concentrations for Mo, Ni and Al cermets, respectively. The ramp I-V curves show a constant displacement current equal to $C_1 \frac{dV_g}{dt}$ (where C_1 is the insulator stack capacitance) plus a non-ohmic current component associated with charge injection into and transport across the oxide layer at higher voltages.[9] The magnitude of the applied gate voltage needed to initiate the electron injection into the oxide decreases as the percentage of metal concentration in the cermet increases. This behavior could be associated with the presence of larger and/or more irregularly shaped metal grains at the SiO_2 - cermet interface as the metal content in the cermet increases. The non-ohmic current component in the ramp I-V curves has a characteristic Fowler-Nordheim behavior as illustrated in Fig. 4 where $J/\mathcal{E}^2$ as a function of $1/\mathcal{E}$ is shown for Mo cermets where J is the magnitude of the injected current per unit area ($J = I/A$) and $\mathcal{E}$ is the magnitude of the average electric field. The lines represent a least-squares fit to the experimental data when plotted in the form of $\ln J/\mathcal{E}^2$ as a function of $1/\mathcal{E}$. This type of fit was made to the data in the region of the I-V curves in which electron

trapping is not yet a dominant effect.[9] For example in Fig. 2, only current values in the range from ~ 2×10^{-10} A to ~ 2×10^{-9} A were used. The expression for the magnitude of the current density as a function of the magnitude of the average electric field predicted by the theory of Fowler-Nordheim emission through a triangular barrier is given by

$$J = (e^3 \mathcal{E}^2 / 16\pi^2 \hbar \phi_{eff}) \exp\left[-4(2m^*)^{1/2} \phi_{eff}^{3/2} / 3\hbar e \mathcal{E}\right] \quad (1)$$

where $\hbar$ is Planck's constant divided by 2π, ϕ_{eff} is the effective interface energy barrier height, e is the magnitude of the charge on an electron, and m^* is the effective mass of a tunneling electron (≈ 0.5 of the free electron mass).[4] Therefore, from the slope K of the $\ln J/\mathcal{E}^2$ vs. $1/\mathcal{E}$ curves an effective energy barrier height ϕ_{eff} can be determined as follows,

$$\phi_{eff} = \left[\frac{3\hbar e\, K}{4(2m^*)^{1/2}}\right]^{2/3} . \quad (2)$$

The calculated ϕ_{eff} values for devices with 80% Mo, 60% Al and 60% Ni cermets were 1.46 eV, 1.2 eV and 1.15 eV respectively. This result can be interpreted as a consequence of localized enhancement of the electric field near the cermet-SiO_2 interface. An average field enhancement factor χ can be calculated by replacing $\mathcal{E}$ by $\chi\mathcal{E}$ and ϕ_{eff} by ϕ in Equation (1), and then using Equation (2)

$$\chi = (\phi/\phi_{eff})^{3/2} \quad (3)$$

where ϕ is the energy barrier for the metal - SiO_2 interface with no cermet. The values of ϕ used were 3.4 eV, 3.2 eV, and 3.7 eV for the Mo-SiO_2, Al-SiO_2, and Ni-SiO_2 interface energy barriers, respectively, as determined by both internal photoemission[10] and Fowler-Nordheim tunneling experiments.[4] The field enhancement factor calculated for Mo cermets with 80% metal content is χ=3.7, and for Al and Ni with 60% metal content χ is approximately 4 and 5, respectively. These field enhancement factors are somewhat larger than the maximum χ obtained with Si-rich injectors (~ 2) which have a similar structure composed of

Si and SiO_2. In both cases, the field enhancement mechanism is believed to be associated with the granular nature of the cermets placed between the SiO_2 layer and the contacting electrode (metal grains in one case and Si islands in the other). However, the values of χ obtained for the metal cermets using Equation (3) are in disagreement with those derived from the I-V plots by calculating the ratio of the electric fields required to induce a given current across a device with a cermet injector as compared to a control MOS[9] (for example, see Fig. 1). This behavior would be expected if there is a large variation of metal particle size, density, and/or grain shape at the cermet-SiO_2 interface. For example, the sharpest grains would control injection at the lowest applied voltages; however, at higher voltages localized electron trapping in the SiO_2 near the sharpest grains would screen out their effect and injection from other grains would tend to dominate the current measured in the external circuit.

In conclusion, the use of granular metal films as injector layers into wide band gap insulators results in electron injection at lower average electric fields than those commonly needed for electron injection directly from the metal into the insulator. This phenomenon is primarily associated with the granular, two phase nature of the injector layer and the interface it forms with the underlying SiO_2 layer. The lowering of the average electric field required for electron injection into the insulator is caused by a geometrical enhancement of the electric field near the injector-insulator interface due to the irregular shape of the metal grains. The increase of the electric field enhancement with metal content in the injector is suggested to be associated primarily with an increase in the size and shape irregularity of the metal grains. The increasing electrical conductivity of the cermet itself with increasing metal content also decreases the electric field in the cermet and increases the electric field in the SiO_2 layer. However, this effect is assumed to be small because of the extremely good insulating properties of the SiO_2 layer.[11]

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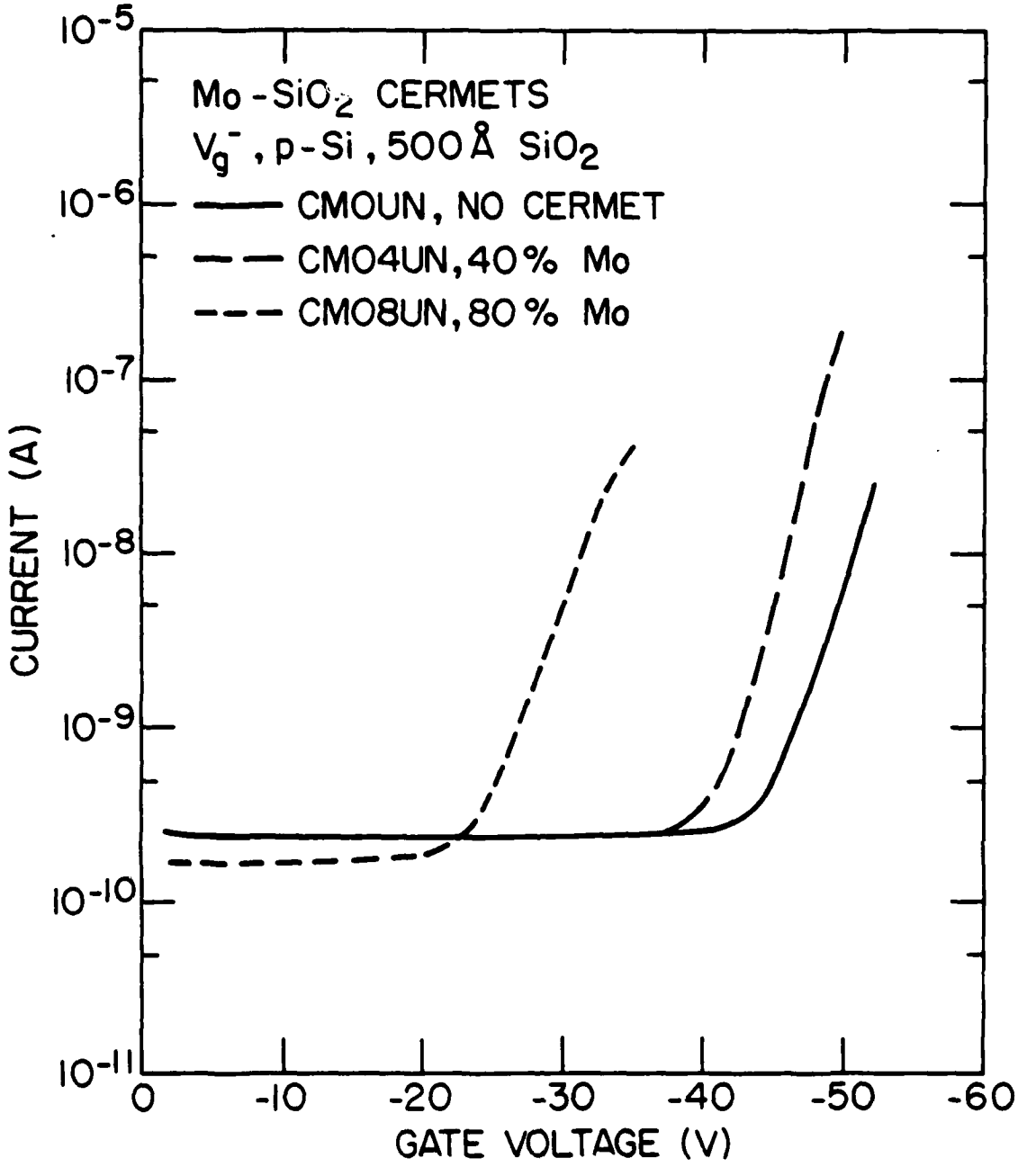
Figure Captions

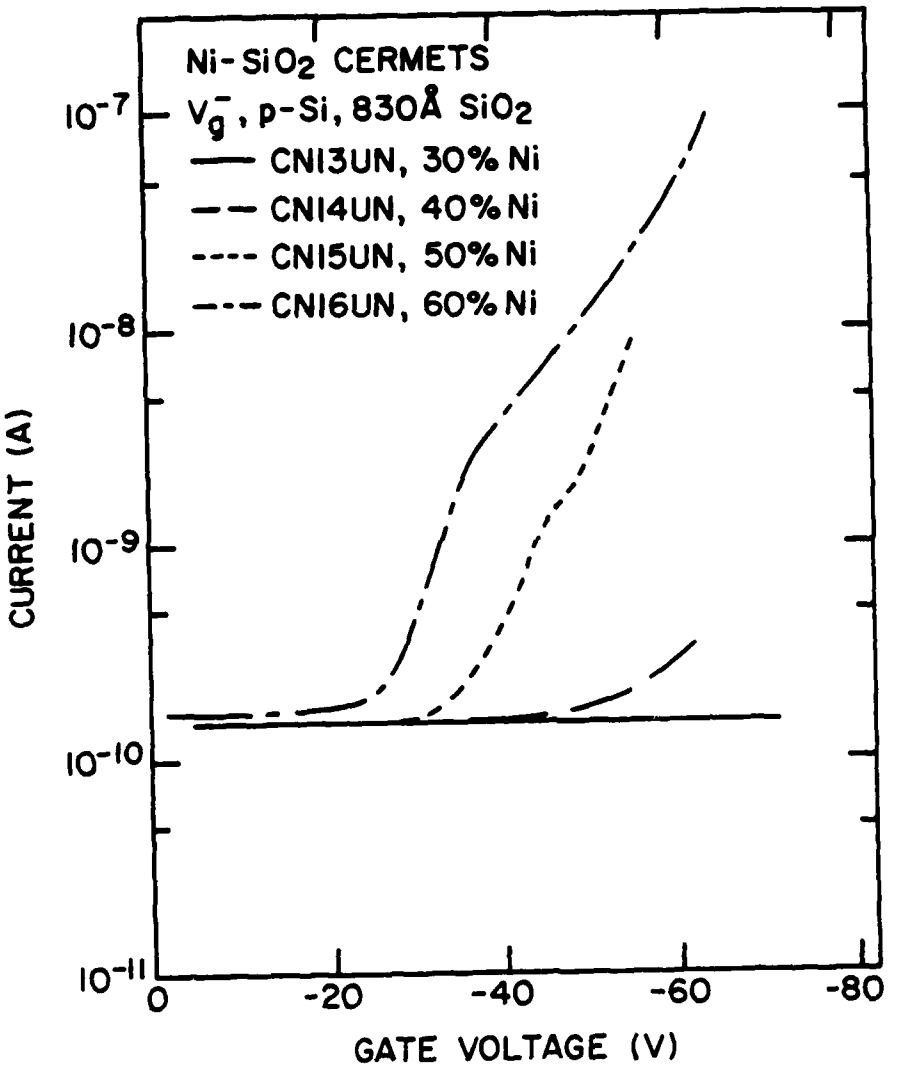
Fig. 1. Ramp I-V characteristics for a metal-cermet-oxide-semiconductor (MCOS) structures incorporating Mo-SiO_2 cermets. The solid line is the I-V curve measured for an MOS structure in which the metal electrode is a layer of Mo. The dashed lines are I-V characteristics of structures involving cermets with the noted metal concentration.

Fig. 2. Ramp I-V characteristics for MCOS structures incorporating Al-SiO_2 cermets. The different curves illustrate the difference in the electron injection characteristics for different metal concentrations in the cermets.

Fig. 3. Ramp I-V characteristics for MCOS structures incorporating Ni-SiO_2 cermets. The different curves illustrate the difference in the electron injection characteristics for different metal concentrations in the cermets.

Fig. 4. The magnitude of the current density over the square of the magnitude of the average electric field as a function of the inverse of the magnitude of the average electric field for structures involving Mo/SiO_2 cermets. The linear behavior of this plot indicates Fowler-Nordheim tunneling as an electron injection mechanism. The solid lines represent least square fits to the experimental data.


Mo - SiO2 CERMETS
Vg⁻, p-Si, 500 Å SiO2
CMOUN, NO CERMET
CMO4UN, 40% Mo
CMO8UN, 80% Mo
CURRENT (A)
10-5
10-6
10-7
10-8
10-9
10-10
10-11
0
-10
-20
-30
-40
-50
-60
GATE VOLTAGE (V)


Ni-SiO2 CERMETS
Vg-, p-Si, 830Å SiO2
CNI3UN, 30% Ni
CNI4UN, 40% Ni
CNI5UN, 50% Ni
CNI6UN, 60% Ni
CURRENT (A)
10-7
10-8
10-9
10-10
10-11
0
-20
-40
-60
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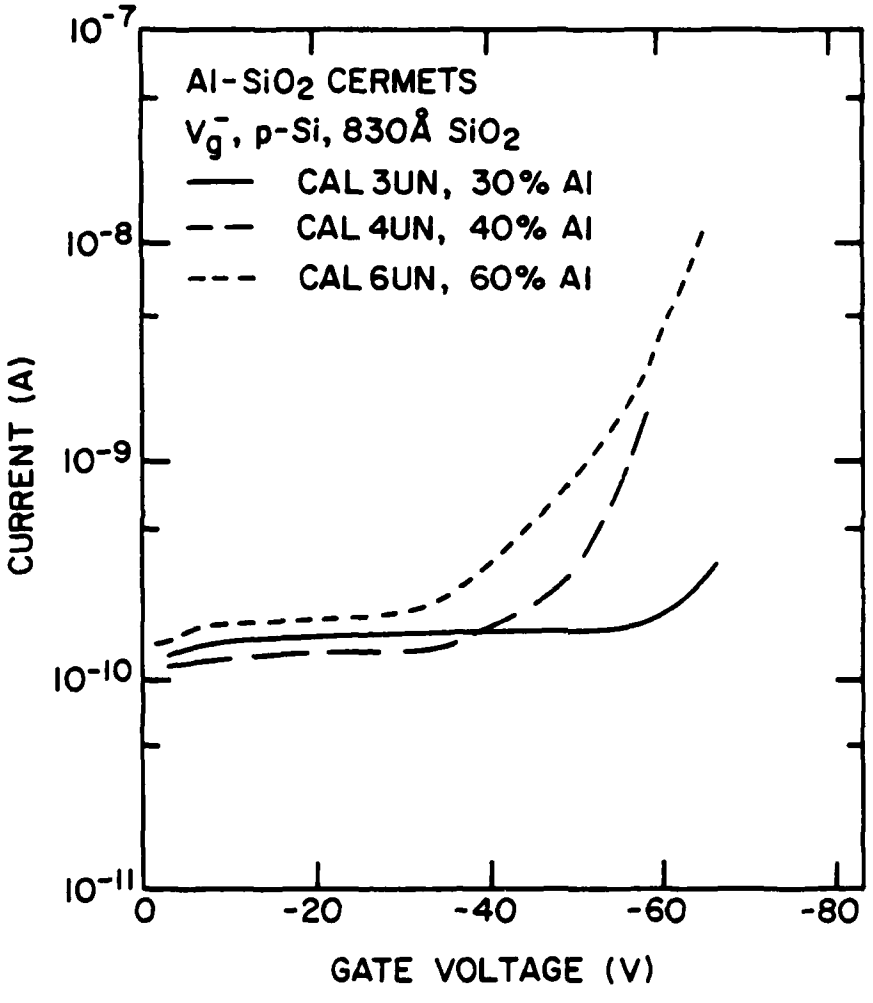
GATE VOLTAGE (V)


Al-SiO2 CERMETS
Vg-, p-Si, 830Å SiO2
CAL 3UN, 30% Al
CAL 4UN, 40% Al
CAL 6UN, 60% Al
10-7
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CURRENT (A)
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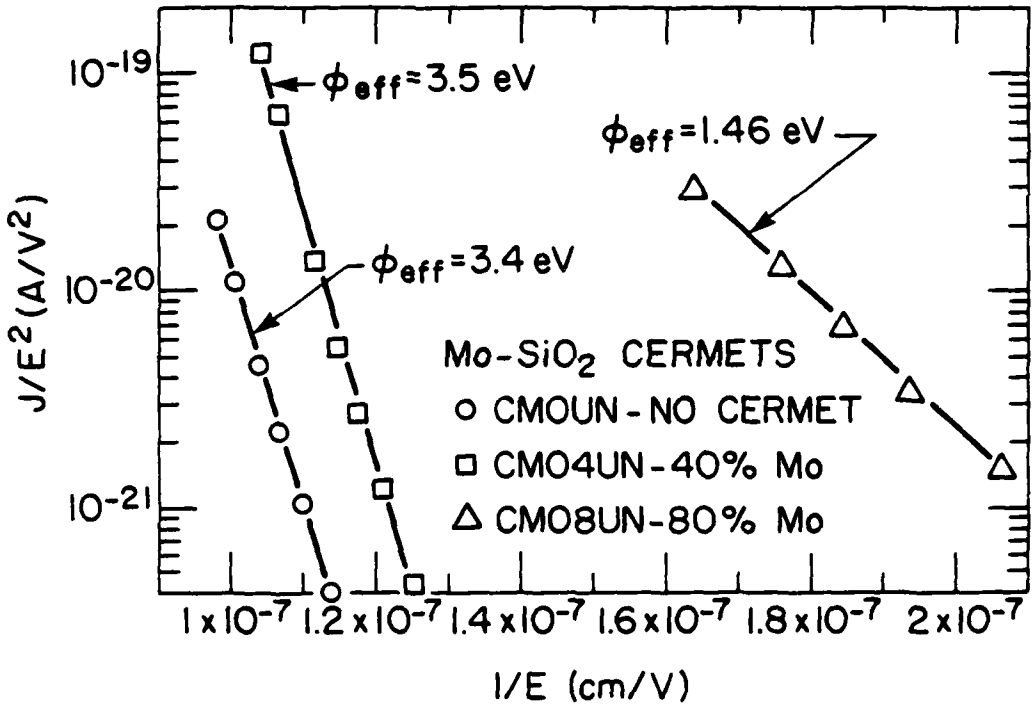
GATE VOLTAGE (V)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J/E^2 (A/V^2)
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ϕ_{eff}=1.46 eV
ϕ_{eff}=3.4 eV
Mo-SiO_2 CERMETS
○ CMOUN - NO CERMET
□ CMO4UN - 40% Mo
△ CMO8UN - 80% Mo
1×10^{-7} 1.2×10^{-7} 1.4×10^{-7} 1.6×10^{-7} 1.8×10^{-7} 2×10^{-7}
1/E (cm/V)

Study of Charge Trapping as a Degradation Mechanism in Electrically-Alterable Read-Only-Memories *

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ABSTRACT

Charge trapping in the intervening oxide layers of electrically-alterable read-only memories (EAROMs) has been studied for different device configurations incorporating a dual electron injector structure (DEIS). The degradation of the write/erase capability of these devices is associated with electron capture in neutral trapping centers present in both chemical-vapor-deposited and thermal oxides. Annealing the exposed DEIS stack at 1000°C in N_2 results in better cycling capability. The dominant traps in unannealed samples were found to have capture cross sections of $\sigma_{c_{ox}} \approx 10^{-16} - 10^{-17}$ cm^2 while those in annealed samples have $\sigma_{c_{ox}} \approx 10^{-17} - 10^{-18}$ cm^2.

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I. Introduction

The ability for extended write/erase cycling on electrically-alterable read-only-memories (EAROMs) is limited by the charge trapping phenomena in the intervening insulating layers[1-5]. Previous work[1-3] on EAROM structures involving chemically-vapor-deposited (CVD) SiO_2 layers in a dual-electron-injector-structure (DEIS) stack have shown that the capability to shift the threshold voltage V_T of the device by charging or discharging a poly-crystalline Si (poly-Si) floating gate starts degrading after approximately 10^3 – 10^4 cycles. This degradation is caused by charge build up in the intervening CVD silicon dioxide layer of the DEIS stack (which separates the control and floating poly-Si gates) due to capture of electrons in energetically deep trapping centers with capture cross sections $\sigma_{c_{ox}} \approx 10^{-16}$ – 10^{-17} cm^2 [6,7]. These traps have been associated with the presence of water related impurities in the oxide.[8,9] In particular, measurements of infrared absorption in thermal SiO_2 films indicate that SiOH and H_2O groups might be associated with traps with electron capture cross sections of the order of 10^{-17} cm^2 and 10^{-18} cm^2, respectively.[10] In general, it has been found that the electron trapping characteristics in thin SiO_2 films are influenced by processing parameters such as high temperature (1000°C) post-oxidation annealling in N_2 and low temperature (400°C) post-metallization annealling in N_2 or forming gas.[11,12,13] In the present work, an annealing treatment at 1000°C for 30 min in N_2 of the DEIS stack is reported to reduce the effective capture cross section for electron trapping by about one order of magnitude. This annealing treatment, consequently allows for an increase in the write/erase cycling capabilities of the EAROM devices by one to two orders of magnitude.

II. Experimental Details

The EAROM devices were fabricated on 0.5 Ω-cm <100> p-type silicon substrates using a self-aligned double poly-Si process previously described by DiMaria, et al.[3]. In the present work, 3-port and 4-port devices[4] were tested. Figure 1 illustrates schematically these two types of devices. The writing or erasing of these devices is achieved by applying a square-

wave voltage pulse of the appropiate polarity to the single control gate in the case of 3-port devices. For 4-port devices, the structure is written by either applying a positive voltage to the gate with capacitance C_3 while the gate with capacitance C_1 containing the DEIS stack is at ground potential, or applying a negative voltage to the DEIS gate with the gate with capacitance C_3 at ground. These two situations are not equivalent.[3] Erasing the 4-port devices is performed by applying a positive voltage to the DEIS gate and grounding the gate with capacitance C_3. In this study, the DEIS stack was also incorporated under the gate with capacitance C_3 in the 4-port devices for simplicity in the fabrication process, which allows one less masking level. However, this is not necessary and in fact imposes limitations on the magnitude of the threshold voltage shifts ΔV_T ($\Delta V_T = V_T - V_{T_i}$ where V_{T_i} is the threshold voltage of a device with the floating gate in an uncharged state) that can be achieved as will be discussed below. The thicknesses of the intervening oxides in the DEIS stacks were 100 Å for DEIS II2-C1,E,F and MDT-DIS3-B, 150 Å for MDT-DIS2-B, and 200 Å for DEIS II2-B. The oxide thickness for the single electron injector structures[3] (SEISs) on wafer MDT-113-C′ was 200 Å. The Si-rich SiO_2 injectors thicknesses were in the range of 100 Å to 1000 Å. Top and bottom injectors were fabricated under deposition conditions to produce equivalent thicknesses and composition. Injector thicknesses were 90 Å, 100 Å, 150 Å, and 1000 Å on devices from wafers MDT-113-C′, MDT-DIS3-B, DEIS II2-B,C1 and MDT-DIS2-B, and DEIS II2-E,F, respectively. After the DEIS stack was deposited, some devices were given a 1000°C anneal in a nitrogen ambient for 30 min. For all devices from the DEIS II2 series of wafers, the gate oxide was thermally grown from the Si substrate to a thickness of 650 Å. MDT-113, MDT-DIS2, and MDT-DIS3 wafers had thermal gate oxide thicknesses of 435, 290 and 100 Å, respectively.

The written or erased state of the floating gate was determined by measuring the threshold voltage V_T required to induce electron current flow between the source and drain I_D as a function of the applied gate voltage V_g. The I_D versus V_g curves were measured with 100 mV applied to the drain and with the source and substrate at ground potential. A voltage ramp

with adjustable amplitude and ramp rate was used to supply the gate voltage. The current was measured with a Keithley Model 427 fast current amplifier. The voltage ramp and the current amplifier were coupled through a comparator circuit which reset the voltage ramp at a preset value of I_D. The I_D vs. V_g curve was displayed on a storage oscilloscope. The complete measurement of the I_D vs. V_g curve could be performed in approximately 2 msec. This characteristic of the measurement system was important to insure minimum perturbation of the charge state of the floating gate during the read operation. The write/erase operation was performed with voltage pulses supplied by two Hewlett Packard pulse generators Model 214A. The width of the pulses used were in the range of 5 ms to 500 ns.

III. Results and Discussions

The change in the threshold voltage shift $\Delta(\Delta V_T) = \Delta V_T(t) - \Delta V_T(0)$[4] as a function of the magnitude of the write/erase voltage was measured for all the devices studied. Figure 2 illustrates the characteristic behavior of the magnitude of $\Delta(\Delta V_T)$ as a function of write/erase voltage magnitude. The lines represent the behavior predicted by a computer simulation.[4] The agreement between the experimental results and the simulation is good at low voltages. However, the experimental curve rolls over and saturates at higher voltages deviating considerably from the predicted behavior. The saturation of $\Delta(\Delta V_T)$ at a maximum amount of charge which can be stored on the floating gate is due to the internal field in the DEIS stack reversing and becoming large enough to turn on the DEIS injectors after the write/erase pulse is over and the gate is grounded. Either excess electrons on the floating gate are leaked back to the top control gate after writing, or excess ionized donors are neutralized by electrons injected from the top control gate after erasing in the case of 3-port devices. For a 4-port device an additional mechanism either contributes to/or controls the saturation of $\Delta(\Delta V_T)$. If the magnitude of the write/erase pulse is large enough, the DEIS stack under the larger area gate with capacitance C_3 (see Fig. 1) is turned on and either leaks off excess electronic charge being injected onto the floating gate back to this control gate during the write operation, or

injects electronic charge onto the floating gate as it is being removed during the erase operation. This additional mechanism for perturbation of the charge on the floating gate for the 4-port devices is due to the presence of the DEIS stack under the gate with capacitance C_3. It can be minimized by adding one masking step in the processing, and making the insulator under this gate only SiO_2 as depicted in Fig. 1c. The asymmetry of the saturation level of $\Delta(\Delta V_T)$ as illustrated in Fig. 2 is produced by the difference in injection efficiency between the top and bottom injectors.[1,3-5] It should be pointed out that read-perturb effects are not as important as the two mechanisms described above in contributing to the saturation phenomenon. This is because of the fast measurement system used in sensing the I_D vs. V_g characteristics in $\approx$ 2 msec.

The effect of the annealing treatment on the write/erase cycling characteristics of these devices is illustrated in Fig. 3. V_T as a function of the number of write/erase cycles is shown in this figure for two identical devices, except that one device had the DEIS stack annealed at 1000°C in N_2 for 30 min and the other one is unannealed. The threshold voltage window of the annealed device starts collapsing after approximately 10^5 cycles which is about one order of magnitude more cycles than the unannealed device. These cycling characteristics were found to be approximately independent of write/erase voltage pulse width as shown in Fig. 4 where the results of V_T as a function of the number of write/erase cycles is plotted for different write/erase voltage pulse widths. The magnitude of the voltage pulse was adjusted in each case to produce a similar write/erase threshold voltage window.

The charge transferred across the DEIS stack for a given change in the threshold voltage shift $\Delta(\Delta V_T)$ can be calculated if one considers that this change in the shift is caused by the fact that the applied field has to compensate for any change of the charge on the floating gate.[4] Therefore,

$$\Delta Q = - C_R \Delta(\Delta V_T) \qquad (1)$$

where ΔQ is the charge added or removed from the floating poly-Si gate during writing or erasing and C_R is the appropriate gate capacitance under reading conditions.[4] The expression for the gate capacitance used during reading depends on whether the device is a 3-port or a 4-port structure. In the case of a 3-port device, this is given by the low field DEIS stack capacitance

$$C_1^* = \varepsilon_o A_1 \left[l_{o_1} + \frac{\varepsilon_o}{\varepsilon_n}(l_{n_1} + l_{n_2}) \right]^{-1} \quad (2a)$$

For the 4-port device, this capacitance is given by the low field capacitance sum of

$$C_1^* + C_3^* = \varepsilon_o \left[l_{o_1} + \frac{\varepsilon_o}{\varepsilon_n}(l_{n_1} + l_{n_2}) \right]^{-1} (A_1 + A_3) \quad (2b)$$

if both gates with capacitance C_1^* and C_3^* are tied together during reading. A_1 is the area of the smaller DEIS port, A_3 is the area of the larger coupling gate (see Fig. 1), l_{o_1} is the intervening DEIS stack oxide thickness, l_{n_1} and l_{n_2} are the top and bottom injector thicknesses, and $\varepsilon_o = 3.9 \times 8.86 \times 10^{-14}$ F/cm and $\varepsilon_n \approx 7.5 \times 8.86 \times 10^{-14}$ F/cm are the low frequency permittivities of SiO_2 and Si-rich SiO_2, respectively[4]. Read perturb effects are minimized by tying the DEIS and coupling gates together during the read operation. The collapse of the write/erase threshold voltage window is associated with charge buildup in the intervening oxide due to electron capture in energetically deep traps known to be present in CVD oxide layers.[6] The capture cross section $\sigma_{c_{ox}}$ for these traps can be estimated using the relationship[7]

$$\sigma_{c_{ox}} = \frac{q}{J_p \tau_{ox}} \approx \frac{qA_1}{Q_{inj}} \quad (3)$$

where q is the magnitude of the charge on an electron, J_p is the magnitude of the average particle current per unit area flowing across the DEIS oxide layer, τ_{ox} is the time constant associated with electron capture by these traps, and $Q_{inj} \approx J_p A_1 \tau_{ox}$ is the magnitude of the total charge passed across the DEIS stack before the threshold voltage window starts to collapse after n cycles. Combining equations 1 and 2 for n cycles, yields

$$\frac{Q_{inj}}{A_I} = 2n\frac{|\Delta Q|}{A_I} = 2n\epsilon_o\left[l_{o_1} + \frac{\epsilon_o}{\epsilon_n}(l_{n_1} + l_{n_2})\right]^{-1} |\Delta(\Delta V_T)| \quad (4a)$$

for a 3-port device,

$$\frac{Q_{inj}}{A_I} = 2n\epsilon_o\left[l_{o_1} + \frac{\epsilon_o}{\epsilon_n}(l_{n_1} + l_{n_2})\right]^{-1}\left(1 + \frac{A_3}{A_1}\right)|\Delta(\Delta V_T)| \quad (4b)$$

for a 4-port device.

This analysis is applicable to our results as long as the voltage magnitude of the write/erase pulses is such that $\Delta(\Delta V_T)$ is not in the saturation regime (see Fig. 2). If $\Delta(\Delta V_T)$ is saturated, equation 4 will underestimate the total charge transferred across the DEIS stack, and lead to a condition of apparently better cycling capability. However, the window collapse is steeper and usually ends in a destructive breakdown of the DEIS stack at a lower number of cycles than in the case where $\Delta(\Delta V_T)$ is not saturated. An illustration of this phenomenon is shown in Fig. 5 where V_T is plotted as a function of the number of cycles for both cases.

The results of applying the analysis described above to our experimental measurements are summarized in Table I. The results for MDT devices correspond to the analysis of measurements previously reported.[3] These results show, regardless of the particular geometrical configuration, that the threshold voltage window collapse of the unannealed devices is controlled by electron trapping where these sites have capture cross sections of the order of $10^{-16} - 10^{-17}$ cm^2. However, the annealed devices are dominated by traps with $\sigma_{e_{ox}} \approx 10^{-17} - 10^{-18}$ cm^2. These capture cross sections are typical of electrically neutral trapping centers present in both CVD and thermal SiO_2 layers.[6-9] The changes of the electron trapping characteristics with the annealing treatment used here are consistent with previous results on charge trapping studies on MOS capacitors.[6-12] Young et al.[12] have indicated that a 1000°C N_2 anneal after oxidation for about 60 min. will reduce the density of neutral traps present in a thermal oxide film. The exact mechanism for the changes induced by the annealing are not well understood. However, it has been suggested that water outdiffusion coupled with

rearrangement of the water impurities (OH converting into H_2O groups) is responsible for the observed changes.[10,12]

IV. Conclusions

The dominant mechanism of degradation in EAROMs which use a DEIS stack for charge transfer is caused by trapped charge buildup in the intervening oxide layer of the DEIS stack due to electron capture into neutral traps. These traps presumabily are the same water related traps previously characterized in MOS structures. It has been demostrated that the number of write/erase cycles can be increased up to two orders of magnitude more than previously reported in this type of device (see Fig. 3) by annealing the exposed DEIS stack in N_2 at 1000°C for 30 min. After the poly-Si gate is deposited on top of the DEIS stack, further high temperature processing does not largely affect the electron trapping characteristics in the intervening oxide. The net effect of the annealing treatment of the exposed DEIS stack appears to be that of driving water impurities out of the intervening oxide layer. This process is inhibited once the poly-Si layer is deposited on the DEIS stack. These results are in agreement with previous work on CVD and thermal oxides in MOS capacitors.[6,12]

The magnitude of the threshold voltage shift ΔV_T or the change in ΔV_T is limited by the internal field generated by the charge stored on the floating gate. ΔV_T or $\Delta(\Delta V_T)$ essentially saturates after the internal field becomes large enough to "turn on" electron injection to or from a control gate. The operation of EAROM devices under saturation of ΔV_T or $\Delta(\Delta V_T)$ will give an additional number of cycles before threshold voltage window collapse. However, larger voltages are required to write or erase the device, and the basic problem of charge buildup in the oxide layer has not really been solved. The analysis described for trap characterization in EAROM structures can be applied in general to any SiO_2 structure where electrons are passed back and forth uniformly through the oxide layer to charge or discharge a floating gate. It appears from this study and the work of S.K. Lai et al.[13] that for the best possible case the maximum number of cycles will be limited to $\lesssim 10^7$ because of electron

trapping in SiO_2. If more cycles are needed, other materials which minimize trapped space charge buildup in the insulator will have to be found.

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Table I. Analysis of Threshold Voltage Window Collapse

DEVICE	TYPE	$\lvert\Delta(\Delta V_T)\rvert$ [volts]	n [#cy]	$\lvert Q_{inj}/A_I\rvert$ [coul/cm^2]	
DEIS II2-C1-16	3-port,An.	7	5×10^3	1×10^{-2}	$\sigma_{C_{ox}} \simeq 10^{-17} - 10^{-18}$ cm^2
DEIS II2-C1-17	3-port,An.	4	10^4	1×10^{-2}	
DEIS II2-C1-21	4-port,An.	3.7	10^4	9×10^{-2}	
DEIS II2-F-21	3-port,An.	7.4	10^5	5×10^{-2}	
DEIS II2-E-21	3-port,Unan.	7	10^4	4×10^{-3}	$\sigma_{C_{ox}} \simeq 10^{-16} - 10^{-17}$ cm^2
DEIS II2-B-20	4-port,Unan.	4	10^2	7×10^{-4}	
DEIS II2-B-21	4-port,Unan.	7	5×10^2	6×10^{-3}	
MDT-113-C′-7	3-port,Unan.	10.5	10^3	3×10^{-3}	
MDT-DIS2-B-7	3-port,Unan.	16	10^3	4×10^{-3}	
MDT-DIS3-B-7	3-port,Unan.	9.5	10^3	3×10^{-3}	

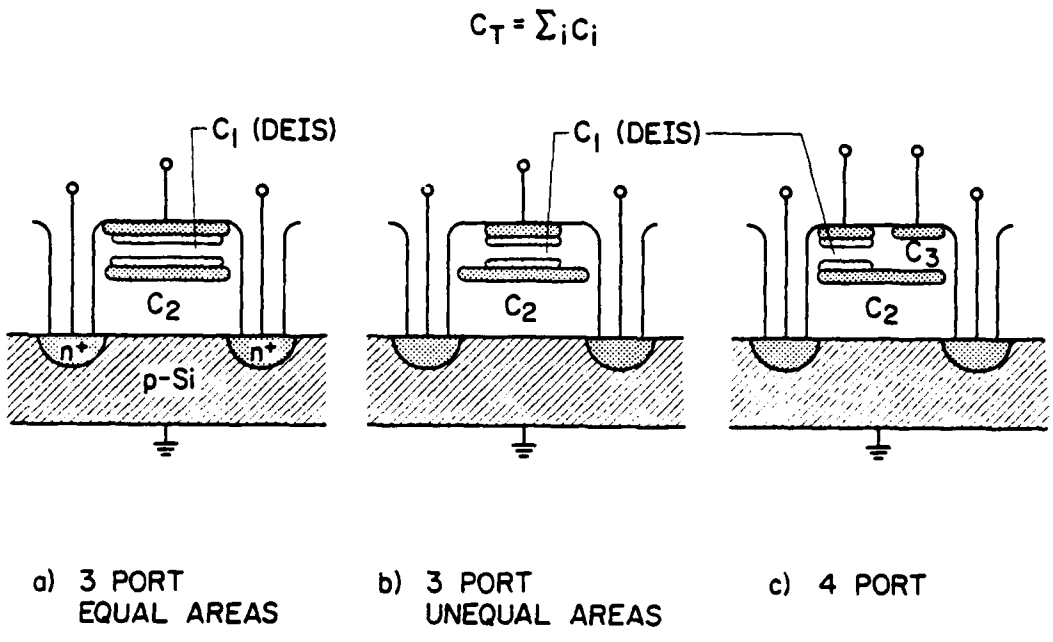

Figure 1. Schematic illustration of the different types of DEIS EAROM structures used in this study. The MDT devices were of the type illustrated in (a) with areas A_1 and A_2 equal to 8.4×10^{-6} cm^2. DEIS II2-C1-16,17, DEIS II2-F-21 and DEIS II2-E-21 devices were of the type illustrated in (b). A_1 and A_2 were 1.1×10^{-6} and 2.7×10^{-6} cm^2 for C1-16, 1.6×10^{-7} and 1.0×10^{-6} cm^2 for C1-17, and 6.8×10^{-7} and 1.1×10^{-6} for F-21 and E-21, respectively. Devices DEIS II2-C1-21 and DEIS II2-B-20,21 were 4-port devices of the type illustrated in (c). A_1, A_2 and A_3 were 7.7×10^{-7}, 1.0×10^{-6}, and 4.8×10^{-6} for C1-21; 1.6×10^{-7}, 5.8×10^{-7}, and 4.2×10^{-6} for B-20; and 5.8×10^{-7}, 1.3×10^{-6}, and 4.4×10^{-6} cm^2 for B-21, respectively.

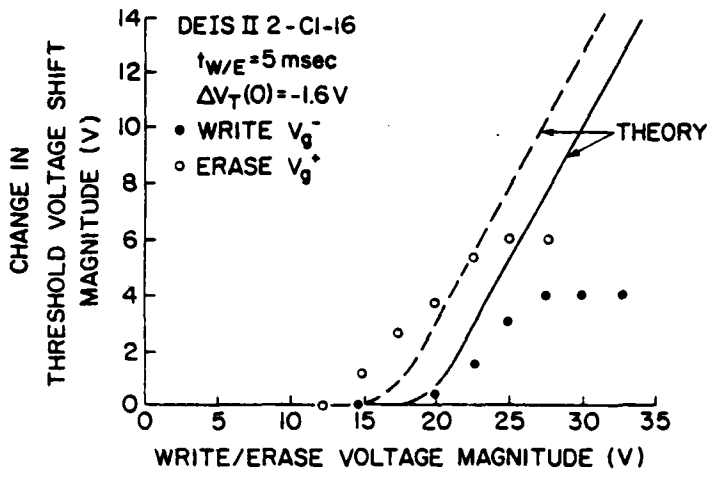

Figure 2. Change in the threshold voltage shift magnitude as a function of the write/erase voltage magnitude. The lines represent the behavior predicted by the computer simulation described in Ref. 4.

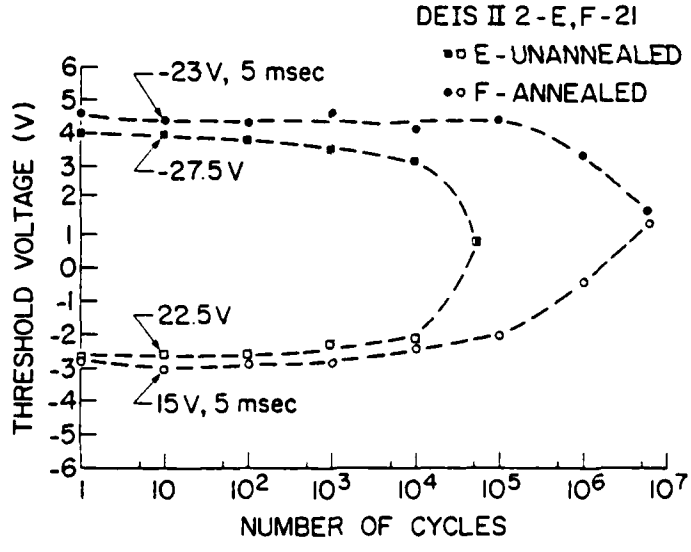

Figure 3. Comparison of the threshold voltage after writing and erasing as a function of the number of cycles for two identical devices, except that one of them (device F) had an annealing treatment in N_2 at 1000°C for 30 min prior to control gate poly-Si deposition.

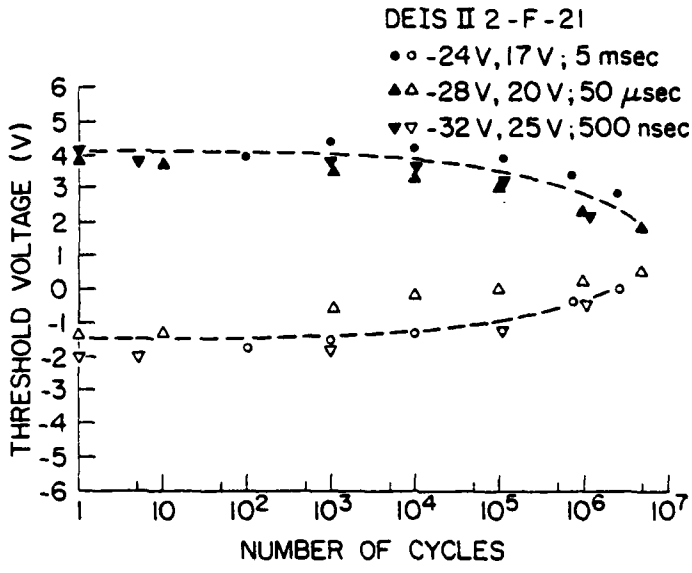

Figure 4. Comparison of the threshold voltage after writing and erasing as a function of number of cycles for different write/erase pulse widths. The voltage amplitude was adjusted to obtain similar shifts of V_T for all cases.

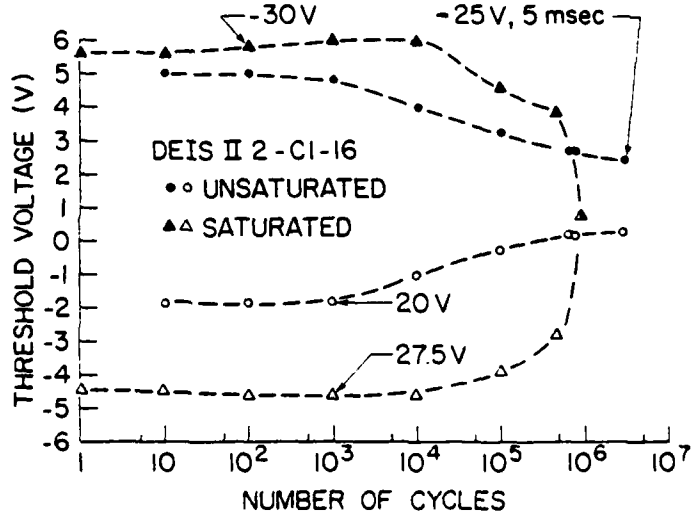

Figure 5. Comparison of the threshold voltage after writing and erasing as a function of the number of cycles for unsaturated and saturated charge state conditions of the floating poly-Si layer.

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SOLID STATE PHYSICS 8 PAGES

Insulator Physics and Engineering: Electrically-Alterable Read-Only-Memory Applications*

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Abstract: Current advances in the study of insulating materials, in particular SiO_2 and Si-rich SiO_2, have led to new types of electronic devices. Si-rich SiO_2, if placed between a contacting electrode and SiO_2, has been demonstrated to give enhanced electron injection into the SiO_2 layer at moderate average electric fields. This phenomenon is believed to be due to localized electric field distortion at the Si-rich SiO_2–SiO_2 interface caused by the two phase nature (Si and SiO_2) of the Si-rich SiO_2 film. Chemically-vapor-deposited layers of Si-rich SiO_2, SiO_2, and Si-rich SiO_2 have been used to charge and discharge floating poly-crystalline Si storage layers in a new type of non-volatile electrically-alterable memory.

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I. Introduction

Several recent publications have demonstrated that high electronic current injection into SiO_2 can be achieved at moderate average electric fields by interposing a thin Si-ri. h SiO_2 layer (50-300 Å in thickness) between SiO_2 and a contacting electrode.[1,2] Data demonstrating this phenomenon are shown in Fig. 1 where a control structure (without the Si-rich SiO_2 layer present) is compared to several structures with Si-rich SiO_2 layers of varying composition. For these structures the SiO_2 was thermally grown from the Si substrate and the Si-rich SiO_2 layer was chemically-vapor-deposited (CVD) from N_2O and SiH_4 gaseous reactants.

The Si-rich SiO_2 material has recently been shown to be composed of at least two phases (Si and SiO_2) using transmission-electron-microscopy (TEM),[3,4] Raman spectroscopy,[5,6] x-ray diffraction,[3,4] and x-ray photoelectron spectroscopy (XPS).[3,4] This two phase nature of the Si-rich SiO_2 is believed to cause the observed electronic current enhancement by locally increasing the electric field near (within 50 Å) the Si-rich SiO_2–SiO_2 interface. The curved surfaces (as compared to the normal planar surfaces of most contacting electrodes) of the last layer of interfacial Si islands in the Si-rich SiO_2 layer are believed to create the field distortion as depicted in Fig. 2 using energy band diagrams. The field-enhanced electron current has been shown to obey a Fowler-Nordheim tunneling mechanism which is highly non-ohmic and strongly dependent on the electric field near the injecting interfaces.[1,7]

Figure 1 shows a structure using one layer of Si-rich SiO_2 under the top gate electrode in which enhanced electron injection is only observed under negative gate voltage polarity. Figure 3 shows two other variations of Si-rich SiO_2–SiO_2 structures which have been demonstrated to give enhanced electron injection for positive (Fig. 3b) gate voltage polarity where the Si-rich

SiO_2 injecting layer is between the Si substrate and SiO_2 or for either positive or negative polarity where a stacked structure of Si-rich SiO_2–SiO_2–Si-rich SiO_2 is sandwiched between the Si substrate and top contacting gate electrode.[8] The structures in Figs. 3a and 3b are called single electron injector structures (SEISs) while that in Fig. 3c is called a dual electron injector structure (DEIS). A previous publication has demonstrated that the sum of the dark current as a function of gate voltage characteristics for the structures in Figs. 3a and 3b essentially add to give those characteristics observed for the structure depicted in Fig. 3c.[8] A distinct asymmetry has been observed between the current-voltage characteristics of DEISs for positive and negative gate voltages in which positive polarity gives higher electron currents for the same applied average electric fields.[8,9] This asymmetry is independent of whether the top gate contact is Al or poly-crystalline Si (poly-Si), or whether the bottom substrate contact is single crystal Si or poly-Si. It is believed to be due to microscopic differences in the Si-rich SiO_2–SiO_2 interfaces of the bottom and top injectors.[8,9]

II. Applications

A. DEIS Memories

A particular application of the electronic properties of a DEIS stack has recently been demonstrated in the area of non-volatile electrically-alterable read-only-memory (EAROM). The basic device configuration of this structure is shown in Fig. 4. It is essentially an n-channel field-effect-transistor (FET) with a floating poly-Si storage layer which is charged or discharged by means of the DEIS stack separating this floating gate from a top control gate electrode.[2,9,10] The voltages used to "write" (put electrons on the floating poly-Si layer by means of the top injector) or "erase" (take electrons off the floating poly-Si layer by means of the bottom injector) the device are always

larger than those used to "read" the FET. The read operation is performed by sensing the electron current flowing from the source to the drain for a constant gate voltage bias (usually $\approx$ +5 V). The internal electric field caused by negative charge on the floating poly-Si layer would shut off the channel and no drain current would be measured. An uncharged or positively charged (due to ionized donors) floating gate would cause the device channel to be turned on for the set reading voltage. Therefore, the charge state of the floating poly-Si layer performs a memory function.

Figure 5 shows typical cycling data for a DEIS EAROM where the FET threshold voltage is used as a measure of the charge state after the device has been written or erased with the values of voltage indicated. These values of write/erase voltage are some of the lowest values ever recorded for an EAROM structure.[9,10] The threshold voltage window in Fig. 5 starts to significantly collapse after approximately 10^4 cycles. This collapse is due to electron trapping on energetically deep sites in the intervening CVD SiO_2 layer.[7,9,11] The internal electric field due to the negative trapped space charge build-up on these sites reduces the electric fields near the injecting Si-rich SiO_2–SiO_2 interfaces of the DEIS.[7,9] The electron trapping sites are believed to be due to bonded OH and H_2O incorporated into the film during deposition.[12] Figure 6 shows that a 1000°C anneal in N_2 for 30 min after DEIS stack deposition reduces the density of some of the trapping sites and allows the device to be cycled somewhat more than one order of magnitude more times.

The DEIS EAROMs described here have been shown to have excellent charge retention at low fields for either positive or negative stored charges on the floating gate.[2,9,10] Retention of electrons is controlled by either thermally activated electron emission from the floating poly-Si (at temperatures $\gtrsim$ 200°C) or Fowler-Nordheim emission from the bottom Si-rich SiO_2 injector at low temperatures and high internal electric fields.[2,9,10] Retention

of positive charges (ionized donors) is controlled by injected electron compensation by either thermal emission (at high temperatures) or by Fowler-Nordheim tunneling (at high fields) from the top Si-rich SiO_2 injector.[9]

DEIS EAROMs have been shown to have excellent breakdown characteristics, particularly when the structure is designed using capacitive coupling considerations to have most of the applied voltage dropped across the DEIS stack.[2,9,10] This phenomenon is due to the ability of the Si islands in the Si-rich SiO_2 layers closest to the contacting electrodes to build up a reversible space charge when a localized point at the contact-insulator interface starts to inject charge due to particulate or roughness at the contacting interfaces.[2,9,10]

The capacitance of the DEIS stack for $\approx$ 13% excess atomic Si in the Si-rich SiO_2 injectors has also been shown to switch from a low to high value with increasing electric field.[1,7] This phenomenon is due to the collapse of the electric field in the Si-rich SiO_2 regions as the Si islands fill up with space charge.[1,7]

DEIS stacks have advantages from the aspect of processing tolerances. It has been shown that the amount of excess Si (for amounts $\gtrsim$ 13% atomic Si) and the thickness of the Si-rich SiO_2 layer (for thicknesses from 100 to 1000 Å) are not very critical in getting reproducible current vs. voltage characteristics.[2] Although high temperature annealing or processing has been shown to convert the amorphous Si islands into crystallites,[4-6] the electrical injection characteristics are again essentially unchanged provided the DEIS stack is not directly exposed to an oxygen containing ambient.[1] These flexible characteristics of the DEIS make it ideally suited for a manufacturing environment.

B. Charge Trapping Studies

Another application of Si-rich SiO_2 injectors has been demonstrated in the area of charge trapping studies in SiO_2 on either sites normally present or purposely introduced.[7] The injector is used as a means of obtaining large electron injection into the SiO_2 conduction band at moderate average bulk SiO_2 electric fields. Usually, electrons are injected at moderate fields by using internal photoemission which requires semi-transparent gate electrodes and ultra-violet light[11] or by avalanche injection from the Si substrate which requires driving the Si into deep depletion with a repetitive pulse train until avalanche multiplication occurs.[11] Using injectors as a source of electrons and ramping the gate voltage at a constant rate yields current-voltage curves with ledges caused by charge trapping.[7] The current position and voltage width of these ledges gives the magnitude of the capture cross section and the total number of traps weighted by a centroid factor.[7] Centroid position can be determined using ledge widths from ramped current-voltage curves for both voltage polarities if DEIS structures are used. If a SEIS structure similar to that depicted in Fig. 3a is used, the centroid position can be obtained from the voltage ledge determined under electron injection from the top Si-rich SiO_2 injector and from the flat-band voltage shift observed using capacitance-voltage measurements before and after the ramped current-voltage measurement.[7] There is an advantage in using Si-rich SiO_2 injectors and ramped current-voltage measurements to determine charge trapping parameters as opposed to the other techniques such as photocurrent-voltage (photo I-V)[11] and capacitance-voltage (C-V) with flat-band voltage tracking.[11] This advantage is speed which allows a large number of capacitors to be studied.

III. Conclusions

Several uses of stacked layers of insulators such as Si-rich SiO_2 and SiO_2 with unique electrical properties have been discussed. Si-rich SiO_2 injectors have been used both in advancing our understanding of the physics of charge trapping in SiO_2 layers and in creating a new type of non-volatile EAROM. Insulator engineering should produce other novel devices in the future as our knowledge of stacked layers of two phase materials and insulators is expanded.

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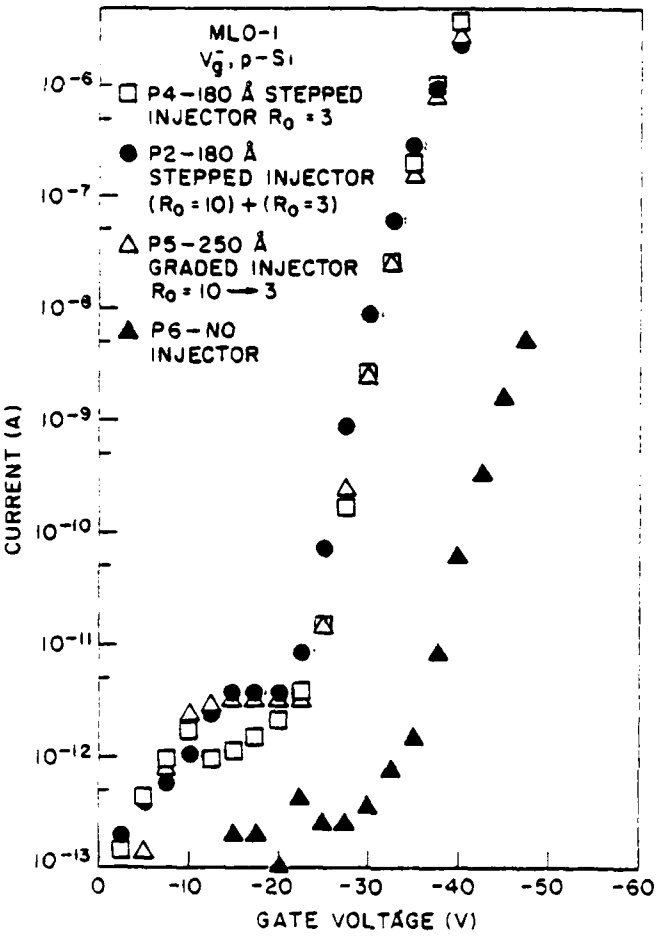

Fig. 1. Point by point magnitude of the dark current as a function of negative gate voltage on MIS structures with various stacks of Si-rich SiO_2 on top of thermal SiO_2. In this measurement, the gate voltage was stepped by −2.5 V starting from 0 V every 20 sec with the dark current being measured 18 sec after each voltage step increase. The Si-rich SiO_2 layer was either stepped or graded with R_o defined as $[N_2O]/[SiH_4]$ as an indicator of the Si content of this layer. R_o from 10 (40% atomic Si) to 3 (46% atomic Si) was used with Si content increasing towards the top metal gate electrode when several layers were stacked on top of the underlying 550 Å thick thermal SiO_2 layer (R_o = 10 + 3) or when a graded layer was used (R_o = 10 → 3). Taken from Reference 1.

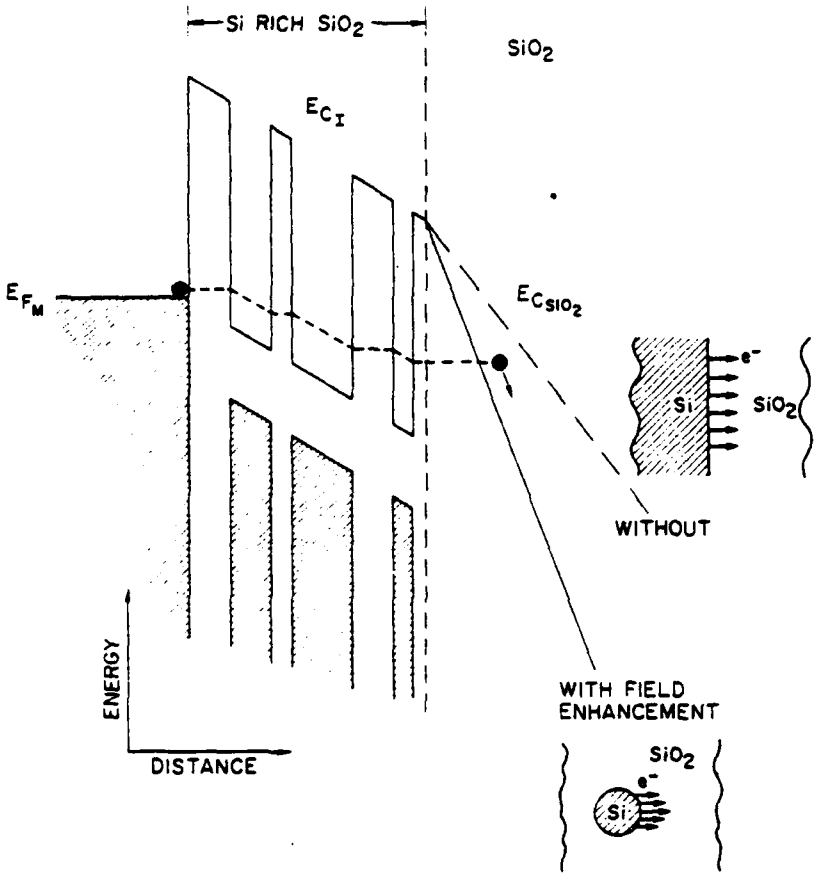

Fig. 2. Schematic energy band representation of conduction in the Si-rich SiO_2 layer via direct tunneling between isolated Si regions in the SiO_2 matrix of this two phase system and subsequent high field injection into the underlying SiO_2 region due to local electric field enhancement caused by the curved surfaces of the Si regions. Electronic Fowler-Nordheim tunneling into SiO_2 from a planar Si surface is shown for comparison. Taken from Reference 2.

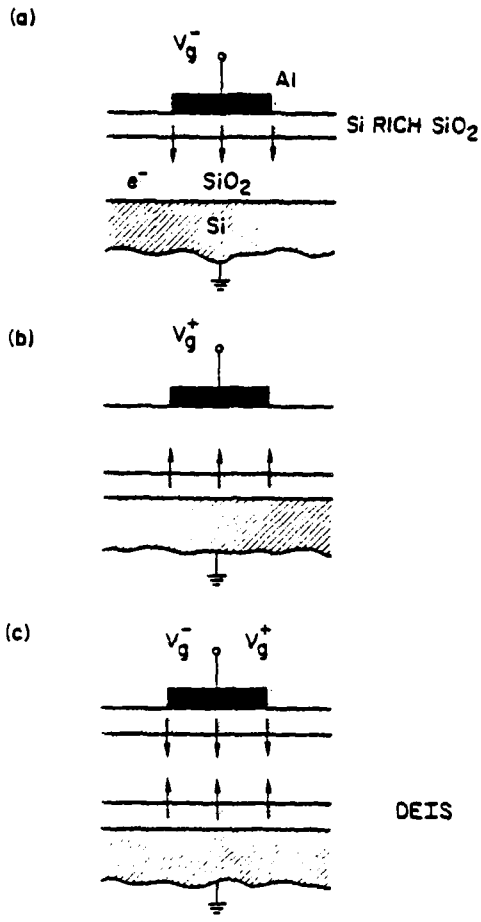

Fig. 3. Schematic representation of a) SEIS with a Si-rich SiO_2 injector on top of the SiO_2 layer and under the control gate electrode, b) SEIS with a Si-rich SiO_2 injector on top of the Si substrate and under the SiO_2 layer, c) DEIS with a Si-rich SiO_2–SiO_2–Si-rich SiO_2 stack sandwiched between the Si substrate and the control gate electrode.

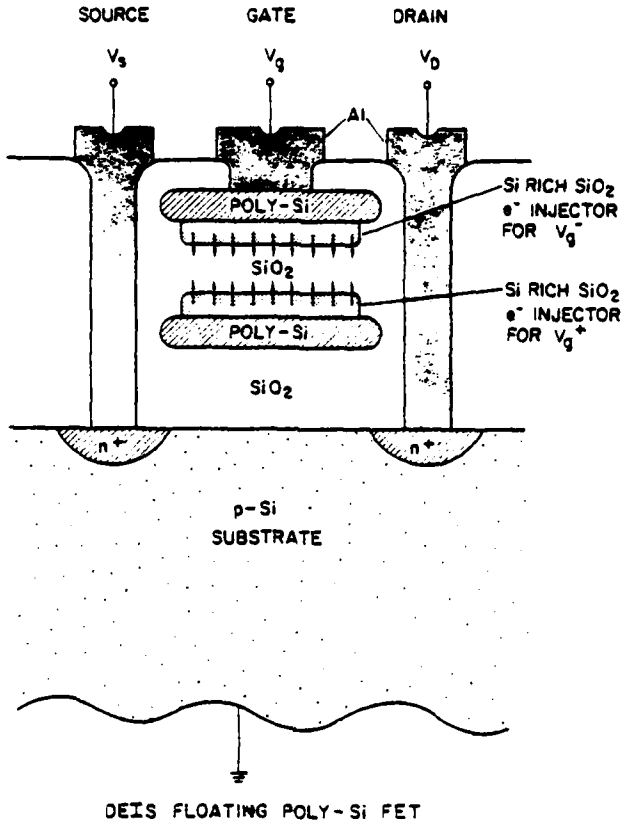

Fig. 4. Schematic representation of a non-volatile n-channel field effect transistor memory using a dual electron injector stack between a control gate and a floating poly-Si layer. Writing (erasing) is performed by applying a negative (positive) voltage, V_g^- (V_g^+), to the control gate which injects electrons from the top (bottom) Si-rich SiO_2 injector to the floating poly-Si storage layer (back to the control gate). Structure is not drawn to scale. Taken from Reference 8.

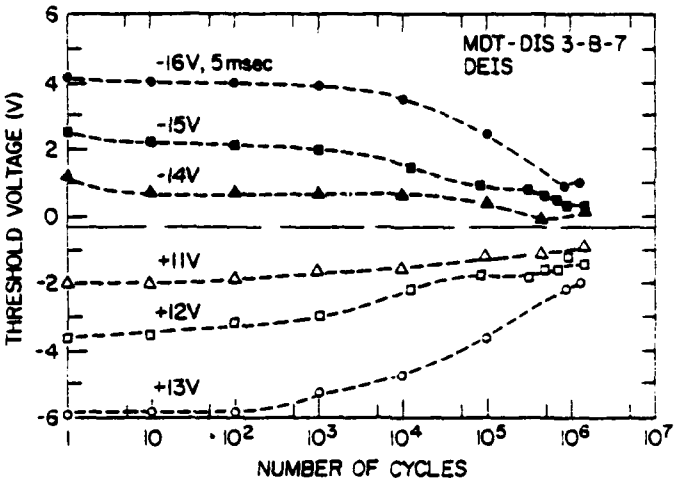

Fig. 5. Threshold voltage after writing and erasing as a function of the number of write/erase cycles for various write/erase conditions on DEIS FETs from wafer MDT-DIS 3-B. Solid and open symbols correspond to the threshold voltage after writing and erasing for 5 msec, respectively. The horizontal dashed line indicates the initial threshold voltage of the as-fabricated FETs before cycling. The DEIS stack in these FETs consisted of deposited layers of 100 Å of Si-rich SiO_2, 100 Å of SiO_2, and 100 Å of Si-rich SiO_2 where the Si-rich SiO_2 layer had 46% atomic Si. The floating and control gates had equal areas of 8.4×10^{-6} cm^2 and the gate oxide from the floating poly-Si layer to the Si substrate was 100 Å in thickness. Taken from Reference 10.

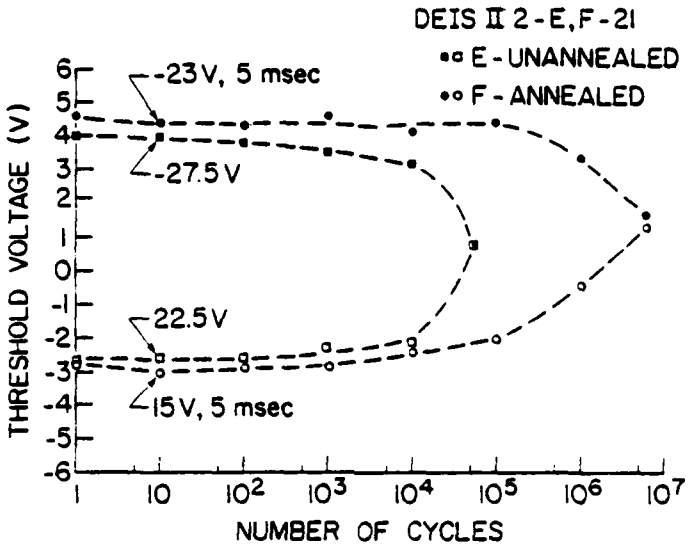

Fig. 6. Comparison of the threshold voltage after writing and erasing as a function of the number of write/erase cycles for two identical DEIS FETs from wafers DEIS II2 E and F, except that one of them (device F) had an annealing treatment in N_2 at 1000°C for 30 min prior to control gate poly-Si deposition. Solid and open symbols correspond to the threshold voltage after writing and erasing for 5 msec, respectively. The DEIS stack in these FETs consisted of deposited layers of 1000 Å of Si-rich SiO_2, 100 Å of SiO_2, and 1000 Å of Si-rich SiO_2 where the Si-rich SiO_2 layer had 46% atomic Si. The floating and control gates had areas of 1.1×10^{-6} cm^2 and 6.8×10^{-7} cm^2, respectively, and the gate oxide from the floating poly-Si layer to the Si substrate was 650 Å in thickness.

Parameter Dependence of RIE Induced Radiation Damage in Silicon Dioxide*

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ABSTRACT: Radiation damage in silicon dioxide films exposed to Reactive Ion Etching (RIE) in CF_4 has been investigated. Capacitance-voltage (C-V) and photocurrent-voltage (photo I-V) techniques were used to monitor charge trapping and location after the films were incorporated into MOS capacitors. Blanket etched films were used to study the trapping characteristics of bulk, neutral, radiation-induced traps as a function of position in the reactor, rf peak-to-peak voltage and pre-RIE high temperature annealing. The trapping characteristics of films etched in a CF_4+H_2 mixture were also studied. Oxide films etched in CF_4+H_2 show reduced trapping when compared with oxides etched in CF_4. The ability of gate electrode materials to shield an underlying oxide during RIE was also tested. It was determined that aluminum and n^+ polysilicon are effective in shielding oxide from RIE induced radiation damage.

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I. Introduction

Reactive Ion Etching (RIE) is a directional, dry etching technique that has been used in our laboratory to fabricate micron dimension FET logic and array chips[1,2]. RIE is used at several levels of processing including definition of recessed oxide isolation, polysilicon gate electrodes, and contact holes to polysilicon and diffused regions. Extensive use of RIE is required for the delineation of fine lines and openings with no undercut of the etch mask. RIE is, however, carried out in a radiation environment; substrates are subjected to bombardment by electrons, ions and photons. For this reason, experiments have been carried out to determine the effect of RIE on the reliability of devices. RIE induced trapping was characterized by exposing a blanket oxide film to RIE, incorporating the etched oxide into an MOS device, and injecting charge into the conduction band of the oxide by avalanche injection. The numbers and cross-sections of the traps, the density of trapped charge, and the centroid of the trapped charge distribution were determined by C-V and photo I-V techniques[3]. Three distinct trapping sites were observed[4]. The first was a buildup of positive charge at the silicon-silicon dioxide interface. These positive trapped charges present a coulombic capture cross-section for electrons in the range of 10^{-12} and 10^{-13} cm^2 and have a density of about 10^{12} postive charges/cm^2. These trapped positive charges are believed to be holes which were generated initially by ionization across the band gap of the oxide. Some of the free positive charges in the silicon dioxide valence band are subsequently trapped at pre-existing sites near the interfaces. The second type of trapping site is created by ion implantation damage within about 5 nm of the surface. These traps are observed only when a non-etching gas such as O_2 is used to clean the surface. Presumably, an etching gas such as CF_4 removes its damage as it is produced leaving only a residual when etching is stopped. The third type of trap is a neutral trapping center. These sites are distributed approximately uniformly throughout the bulk of the oxide. The electronic capture cross-sections of these traps are

between 10^{-14} and 10^{-17} cm^2 and their density is between 10^{11} and 10^{12} cm^{-2}. These traps are very similar to those observed by Aitken, Young, Pan and Ning[5-7] for oxides exposed to much higher energy radiation than in the present case (20-25 KeV X-rays or electrons). In the comparatively low energy environment of RIE, the occurrence of trapping in the bulk suggests, by process of elimination, the involvement of photons which are sufficiently energetic to penetrate the oxide. Ion energies are not sufficient to penetrate the oxide, and energetic electrons would not reach the cathode because of its negative bias. High energy photons, though, would be created in the reactor when secondary electrons which are accelerated across the cathode dark space strike ground planes. Photons generated by secondary electrons in an rf sputtering configuration have been shown to degrade the stability of MOS devices[8]. Secondary electrons vary in energy depending on when they are emitted during the rf cycle, but some may have energies corresponding to the full peak-to-peak voltage. Photon energies, then, could also approach this value. The trapped positive charge and the ion implantation damage were not studied beyond their initial characterization (Table I). The trapped positive charge is annealed at a low temperature of 400°C on the aluminum gated structures used in this study. The implantation damage can be eliminated by dip etching the oxide since the damage is confined to the surface or by avoiding the use of a non-etching gas. The neutral traps, however, are present throughout the bulk of the oxide and an anneal of 600°C or more is required for their removal. Thus, they must be avoided or annealed before aluminum metallurgy is in place.

In the present study, the RIE parameter dependence of the neutral traps was studied. The RIE parameters that were varied include position of substrate in the reactor, rf voltage and composition of etching gas. Finally, the ability of gate electrode materials to shield an underlying oxide from RIE radiation damage was evaluated by etching oxide films masked with aluminum or n^+ polysilicon patterns.

II. Experimental

A. RIE System

The Reactive Ion Etching system used in this work is shown in Fig. 1. The substrates were loaded onto an 18 cm diameter aluminum plate. The aluminum plate was mechanically and electrically connected to the water cooled copper rf cathode. A perforated anode plate which is attached to the grounded chamber was placed 3.3 cm from the cathode in order to prevent backsputtering of aluminum sputtered from the substrate holder. A perforated anode plate was used so that wafers could be monitored visually during etching, and also to ensure an adequate and uniform supply of etchant in the vicinity of the wafers. The chamber was evacuated with a 6 inch oil diffusion pump and then backfilled with 40 sccm CF_4 to establish a dynamic pressure of 3.33 Pa (25 millitorr). During etching, 0.25 W/cm^2 is delivered to the cathode. Under these conditions, the peak-to-peak voltage is 800 V. The dc voltage at the cathode is approximately one half of the peak-to-peak voltage[9]. The etch rate of silicon dioxide in CF_4 is about 50 nm/min.

B. Sample Preparation

Dry silicon dioxide films of 150 nm thickness were grown on boron doped, <100> orientation, 0.1 to 0.5 Ω-cm resistivity p-type silicon substrates. The oxide films were then exposed to a CF_4 or CF_4 + H_2 plasma to etch approximately 50 nm of silicon dioxide. The wafers were then cleaned to remove metals and hydrocarbons from the surface of the oxide in alkali and acid peroxide solutions using a procedure similar to that used by Irene[10], but without HF. Some wafers received a buffered HF dip at this point in order to remove ~10 nm from the surface of the oxide. After cleaning, some wafers were annealed in a N_2 ambient for 30 minutes. Annealing temperatures ranged from 600 to 1000°C. Circular aluminum dots, ~3.5 nm in thickness and 5.2x10^{-3} cm^2 in area, were then evaporated in vacuum from resistively heated tantalum boats or rf heated crucibles. Finally, the backs of

the wafers were stripped and metallized, and a forming gas anneal at 400°C for 20 minutes was carried out.

C. Techniques

To investigate the enhanced electron trapping characteristics of silicon dioxide layers exposed to plasmas in an RIE system, avalanche injection[11,12] and internal photoemission[13-15] techniques were used to inject electrons from the contacts of the MOS structures into the oxide. The experimental apparatus for avalanche injection[16] and internal photoemission[17] have been described in other publications. As the electrons traverse the film in the presence of an applied electric field, some of the carriers are trapped into sites created during RIE. This trapping is not particularly sensitive to the mode of carrier injection: avalanche injection from the silicon or internal photoemission from the aluminum or silicon. The trapping rate is not particularly sensitive to the average field in the oxide layer which is consistent with the weak field dependence of the capture process for radiation induced neutral traps recently reported by Ning[7]. This weak field dependence is in contrast to the strong field dependence of electron capture on trapped holes[3,7,18].

The buildup of this trapped charge is sensed through the internal electric field it creates near the contacts by the capacitance-voltage (C-V)[19,20] and photocurrent-voltage (photo I-V)[18,21,22] techniques which are well described in the literature. The voltage shifts between the C-V curves depend on the product $\bar{x}Q$ where Q is the charge per unit area and $\bar{x}$ is the centroid of trapped charge in the oxide layer measured with respect to the aluminum-oxide interface[19,20]. The voltage shifts between photo I-V data for both positive and negative polarity allow separate determination of $\bar{x}$ and Q[18,21]. The combination of the C-V and photo I-V techniques can also be used to separate silicon-silicon dioxide interface trapping from bulk oxide trapping[18,21,22]. Also by studying charge buildup as a function of time, electron capture cross-sections σ_c and areal trap densities N_t can be determined[3]. These

quantities ($\bar{x}$, Q, σ_c, and N_t) are used to characterize the different traps created by the exposure to RIE plasmas in the following sections. Only a very small amount of trapping was seen for the charging conditions used on samples fabricated in an identical manner, but not exposed to RIE[4]. The results were reproducible for different locations within a sample, and for samples fabricated over a time span of several months.

III. Results and Discussion

A. RIE Parameter Dependence

It was suggested earlier that the neutral traps are created in the relatively low energy environment of RIE by photons. To substantiate this view, substrates were loaded onto the grounded perforated plate with the oxide film facing away from the cathode. In this way, the oxide film is no longer subjected to bombardment by energetic ions. The oxide film is also protected from secondary electrons from the cathode by the silicon substrate. The oxide film is, however, still exposed to photons that are created when secondary electrons strike the walls of the reactor. A plot of the volume density of trapped charge as a function of avalanche injection time (Fig. 2) shows that the oxide etched by RIE and the oxide exposed only to energetic photons show enhanced trapping relative to that measured in the control. Data points are taken at 44 second intervals and so are represented by a solid line. The error bars included for data plotted against an expanded scale in Fig. 7 are representative of data shown in Figs. 2-6.

In the second experiment, the rf power was varied in order to vary the rf peak-to-peak voltage. Etch times were increased as voltage was decreased so that the amount of oxide removed was constant. The purpose of this experiment was to determine whether the introduction of traps exhibited a threshold in the regime of power and pressure that is appropriate for RIE. As can be seen in Fig. 3, enhanced trapping was observed for all oxides

etched by RIE even though rf peak-to-peak voltage was reduced by more than a factor of two, from 730 to 330 V. Thus, radiation damage is not avoided by etching for longer times at lower rf voltages. It is not possible to carry out RIE at lower voltages. RIE requires low pressures to maintain vertical etching and a low pressure discharge could not be sustained at voltages below 330 V. It is possible, however, to reduce voltage if the requirement for directional etching is suspended. For the third experiment, pressure was increased to simulate plasma etching. Oxygen was added to CF_4 so that a direct comparison could be made with oxides etched in a commercial barrel plasma etcher. The pressure of the CF_4+20%O_2 etching gas was increased to 0.5 Torr which results in an rf peak-to-peak voltage of 120 V. The trapping data (Fig. 4) show that neutral traps are not created during plasma etching or during etching under plasma etching - like conditions in the RIE reactor. For completeness, an oxide was etched by low pressure RIE in the CF_4+O_2 mixture to assure that the addition of O_2 was not the significant factor. As expected, this oxide shows the presence of neutral traps with a trap density that is approximately equal to that of an oxide etched in CF_4.

The fourth and last experiment carried out with blanket etched oxide films was to add H_2 to CF_4. This experiment was suggested by speculation that the neutral traps were created by breaking or relaxing bonds in the lattice of the oxide[6]. If correct, the diffusion of atomic hydrogen into silicon dioxide might anneal neutral traps in a way that is analogous to the reduction in dangling bond density in amorphous silicon by atomic hydrogen[23]. The data in Fig. 5 show that the addition of H_2 does lead to a significant reduction in trapped charge when compared with an oxide etched in CF_4 alone. A peak-to-peak voltage of 810 V was measured. This value is slightly higher than that measured during RIE in CF_4. While the effect of adding H_2 is reproducible and consistent with annealing of traps by atomic hydrogen, it was not possible to reduce trap density by introducing hydrogen in other ways.

Trapping was not reduced by exposing oxides to a hydrogen plasma before or after RIE in CF_4 or by annealing oxides in forming gas (90% N_2/10% H_2) at 1000°C before RIE in CF_4.

B. Gate Shielding

The purpose of experiments carried out with blanket oxide films is to understand the nature and parameter dependence of the neutral traps. During FET processing, however, the gate oxide is covered by the material that is used as a gate electrode. With this fact in mind, the ability of polysilicon and aluminum to shield an underlying gate oxide from the introduction of neutral traps was tested.

The procedure used to fabricate the samples begins with the same cleaning and oxidation steps described earlier. After the oxide was grown, a 350 nm thick film of silicon was deposited by chemical vapor deposition on some substrates and then doped n^+ by the deposition and drive-in of $POCl_3$. The polysilicon plus 50 nm of oxide was etched using patterned photoresist to delineate 32 mil diameter dots. On other oxidized substrates, 32 mil diameter, 400 nm thick aluminum dots were evaporated by resistive heating. 50 nm of oxide was then etched by RIE. Appropriate control wafers were included to determine background trapping in the oxide, to provide a reference for the degree of shielding by the gate electrode, and to provide a comparison with wet etching of polysilicon. The data in Fig. 6 show that 400 nm of aluminum does shield the oxide. The shielded oxide exhibits the same increase in trapped charge density as the control, while the unshielded oxide again shows enhanced trapping. The trapping data for oxides covered by polysilicon plus resist during RIE also show that the oxide has been effectively shielded (Fig. 7). The trapped charge density for the reactive ion etched structure is shown on an expanded scale with the trapped charge density obtained for a structure that was wet etched. The two samples show the same low density of trapped charge. In fact, the trapped charge density measured for both samples is

approximately half that measured on similar structures with aluminum electrodes. This reduction is attributed to a decrease in background oxide trapping as a result of the high temperature deposition and doping of the polysilicon films. Other differences in plots of the trapped charge density as a function of the avalanche injection time on the Al-gated controls (compare Figs. 2 and 6 with Figs. 3, 4, and 5) are due to differences in the magnitude of the avalanche current used.

IV. Summary

The parameter dependence of neutral traps introduced during RIE has been investigated under worst case conditins of blanket etching and also with a gate electrode in place. During blanket RIE of silicon dioxide, neutral traps are created. These traps are removed by a 600°C anneal and so are of concern only if an RIE step occurs after aluminum metallurgy is in place. The trap density is reduced by adding H_2 to the etching gas. Neutral traps were not introduced when the reactor was operated under plasma etching like conditions. Finally, it is concluded that oxide is effectively shielded during RIE by a polysilicon or aluminum gate electrode.

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TABLE I: SUMMARY OF TRAPPING CENTER DATA

TRAPPING CENTER	CROSS SECTION (CM^2)	DENSITY (CM^{-2})	SOURCE	ANNEAL T°C
positive charge	10^{-12}-10^{-13}	10^{12}	photons	400
implantation damage	10^{-14}-10^{-18}	10^{13}	ions	1000
neutral center	10^{-14}-10^{-17}	10^{11}-10^{12}	photons	600
background	10^{-17}	10^{12}	-	-

Figure Captions

Fig. 1 Schematic of RIE Reactor

Fig. 2 Volume trapped charge density as a function of avalanche injection time for oxides exposed to RIE on the electrode and on a ground plane. Constant avalanche current = $8x10^{-9}$ amps.

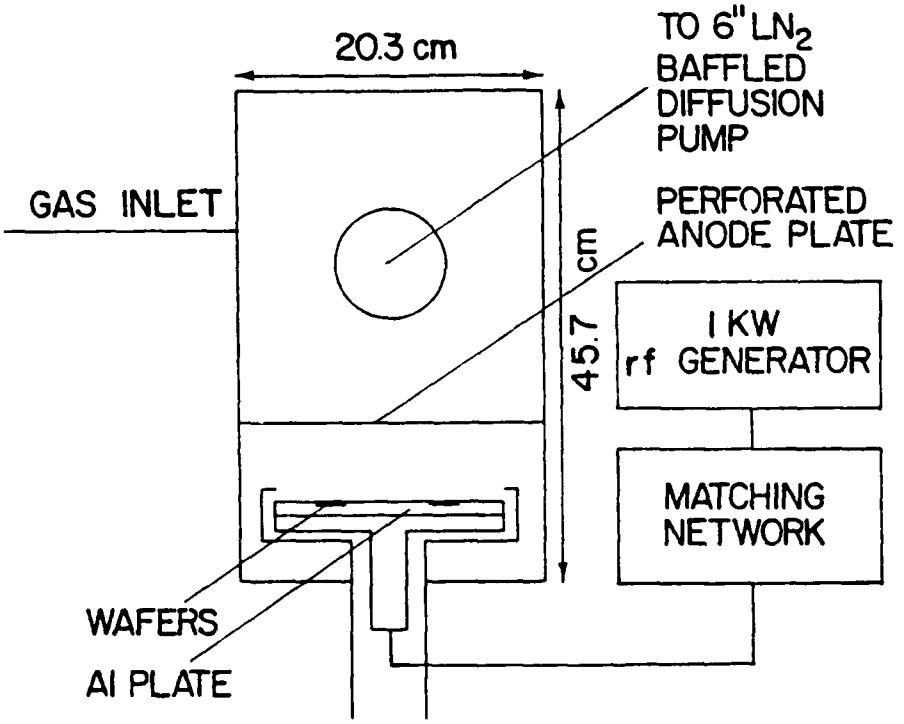
Fig. 3 Volume trapped charge density as a function of avalanche injection time for oxides exposed to RIE with rf peak-to-peak voltages between 730 and 330V. Constant avalanche current = $2x10^{-9}$ amps.

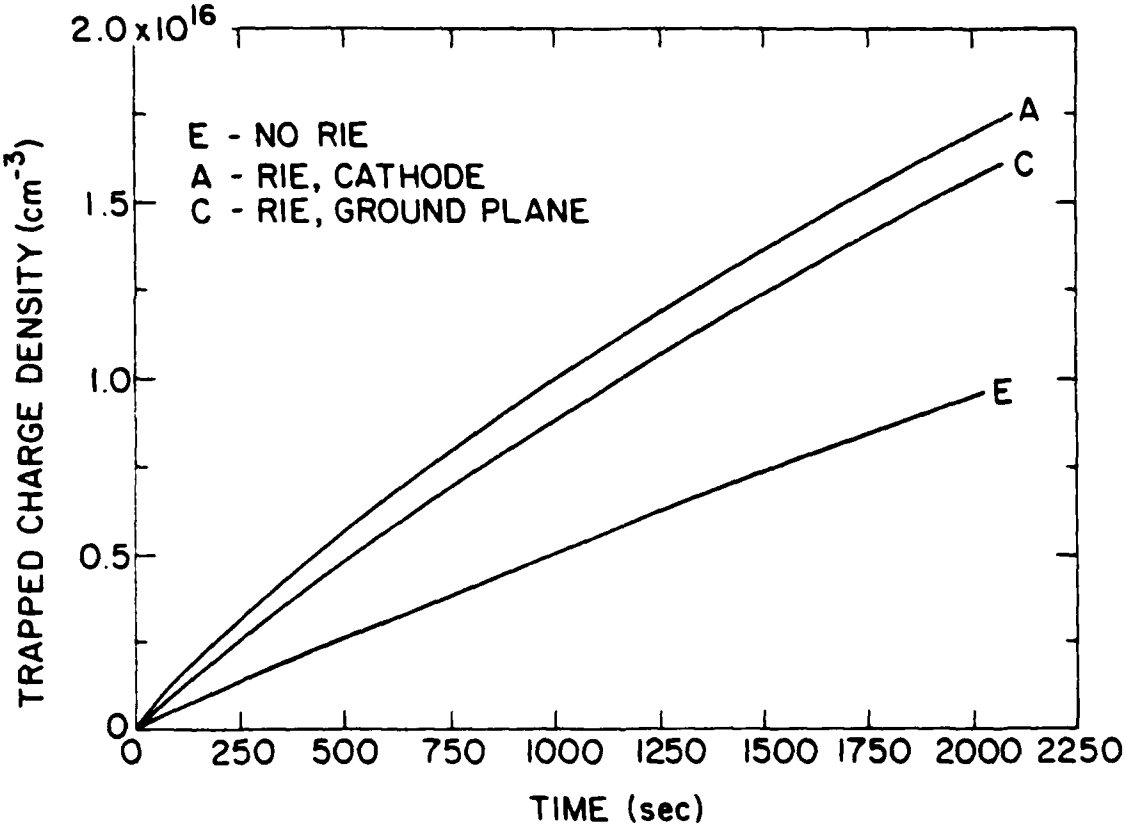
Fig. 4 Volume trapped charge density as a function of avalanche injection time for oxides exposed to RIE in CF_4+O_2 and plasma etching in RIE and barrel-type plasma reactors. Constant avalanche current = $2x10^{-9}$ amps.

Fig. 5 Volume trapped charge density as a function of avalanche injection time for oxides exposed to RIE in CF_4 and CF_4+H_2. Constant avalanche current = $2x10^{-9}$ amps.

Fig. 6 Volume trapped charge density as a function of avalanche injection time for oxides exposed to RIE with and without an aluminum etch mask. Constant avalanche current = $8x10^{-9}$ amps.

Fig. 7 Volume trapped charge density as a function of avalanche injection time for oxide after RIE of polysilicon electrode. Sample in which polysilicon was wet etched serves as a control. Constant avalanche current = $8x10^{-9}$ amps.


20.3 cm
TO 6" LN_2 BAFFLED DIFFUSION PUMP
GAS INLET
PERFORATED ANODE PLATE
45.7 cm
1 KW rf GENERATOR
MATCHING NETWORK
WAFERS
Al PLATE


2.0 x 10^16
1.5
1.0
0.5
0
TRAPPED CHARGE DENSITY (cm^-3)
E - NO RIE
A - RIE, CATHODE
C - RIE, GROUND PLANE
A
C
E
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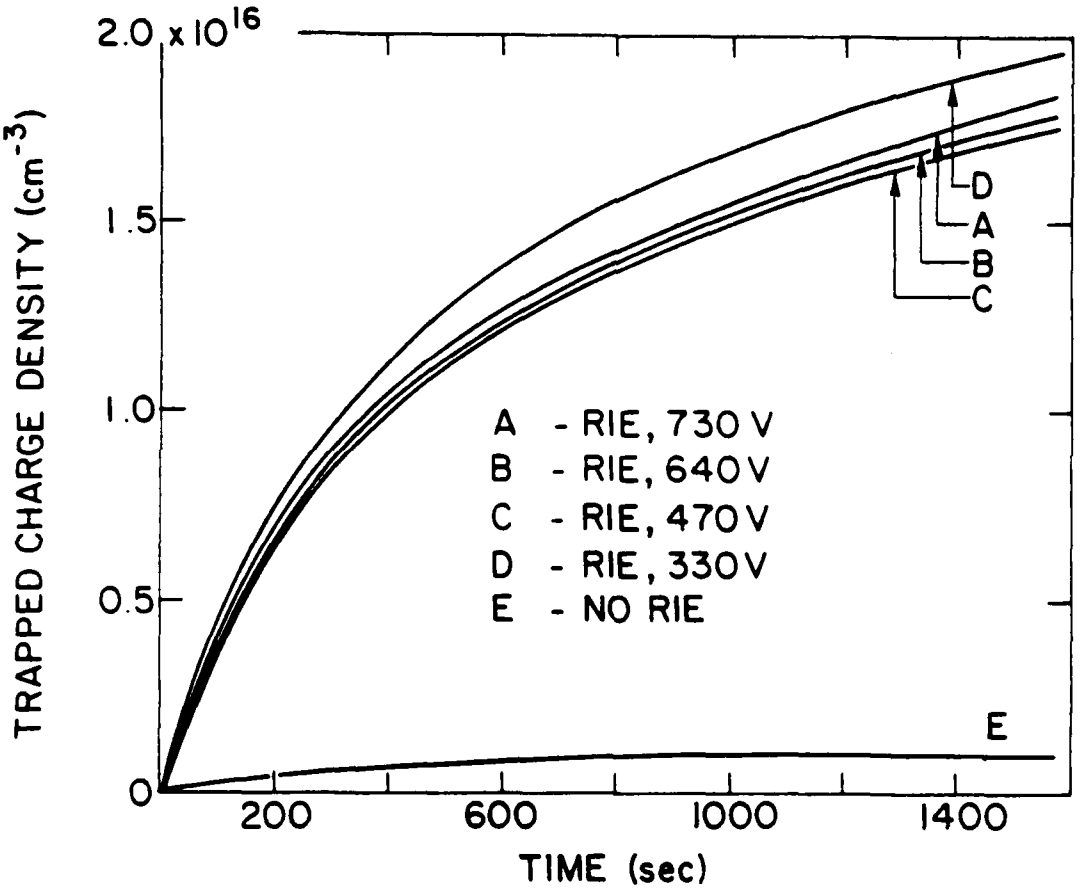
500
750
1000
1250
1500
1750
2000
2250
TIME (sec)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1.0
0.5
0
TRAPPED CHARGE DENSITY (cm^-3)
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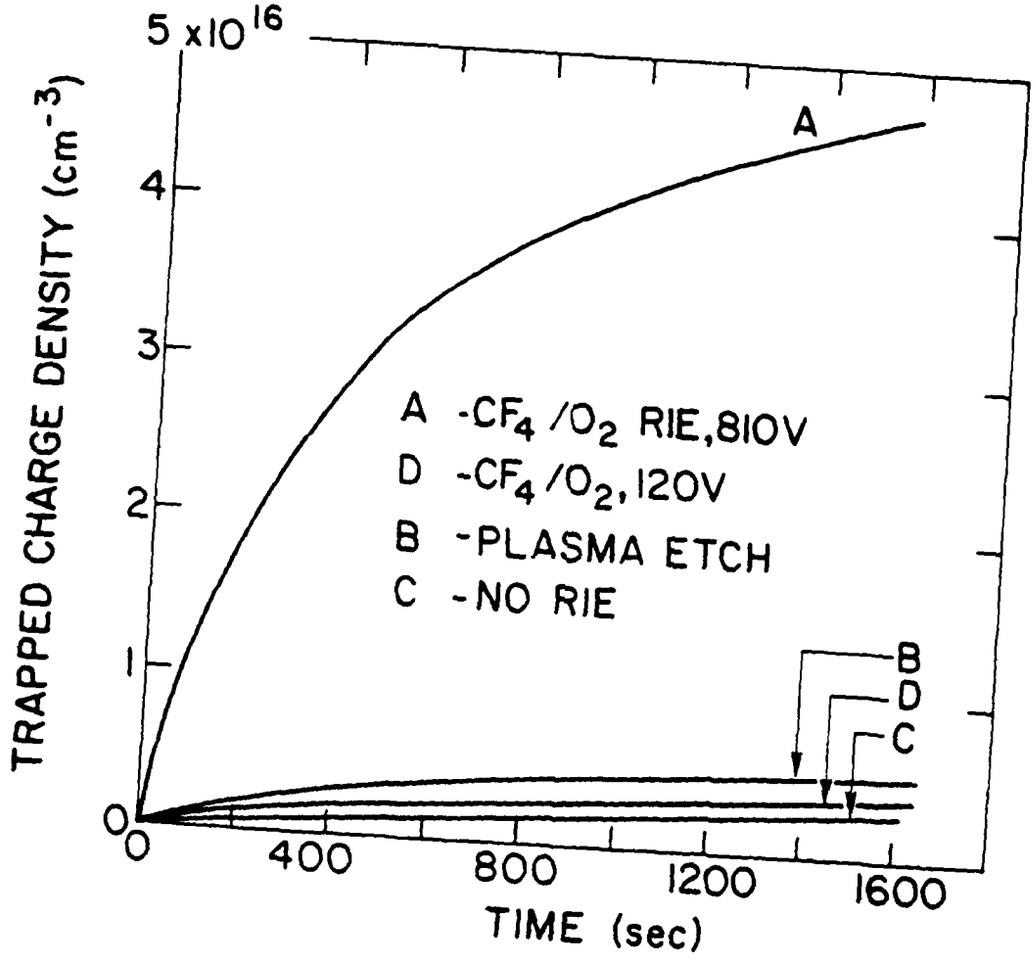
600
1000
1400
TIME (sec)
A - RIE, 730 V
B - RIE, 640 V
C - RIE, 470 V
D - RIE, 330 V
E - NO RIE
D
A
B
C
E


5 x10^16
4
3
2
1
0
0
400
800
1200
1600
TIME (sec)
TRAPPED CHARGE DENSITY (cm^-3)
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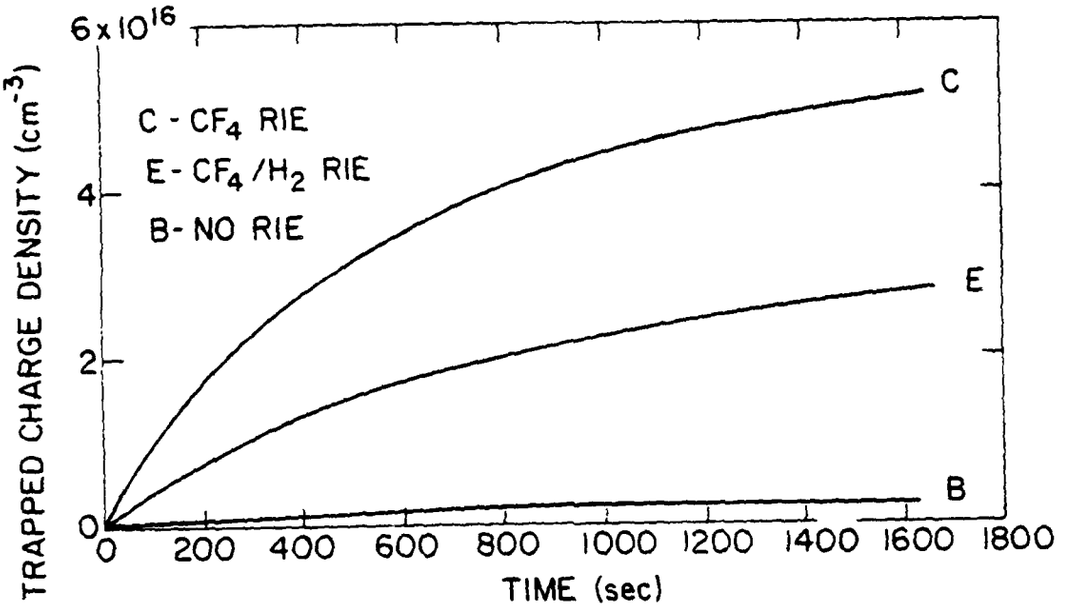
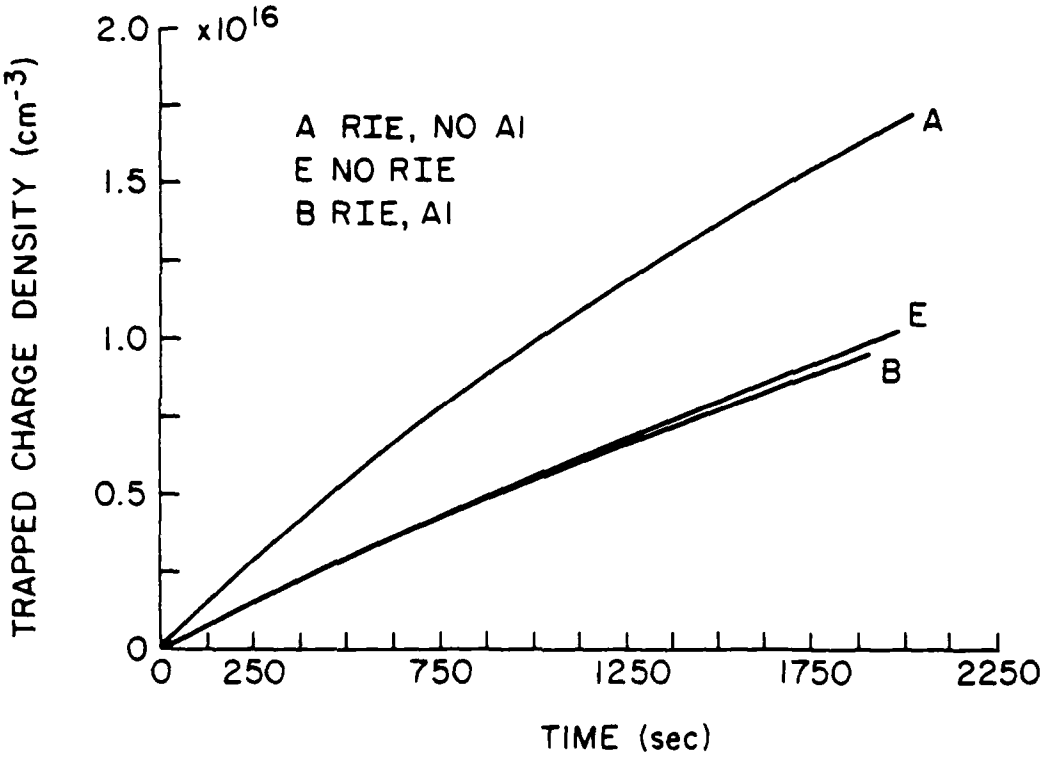
B
D
C
A -CF4 /O2 RIE,810V
D -CF4 /O2, 120V
B -PLASMA ETCH
C -NO RIE


6x10^16
4
2
0
TRAPPED CHARGE DENSITY (cm^-3)
C - CF4 RIE
E - CF4 /H2 RIE
B - NO RIE
C
E
B
0
200
400
600
800
1000
1200
1400
1600
1800
TIME (sec)


2.0
x10^16
1.5
1.0
0.5
0
TRAPPED CHARGE DENSITY (cm^-3)
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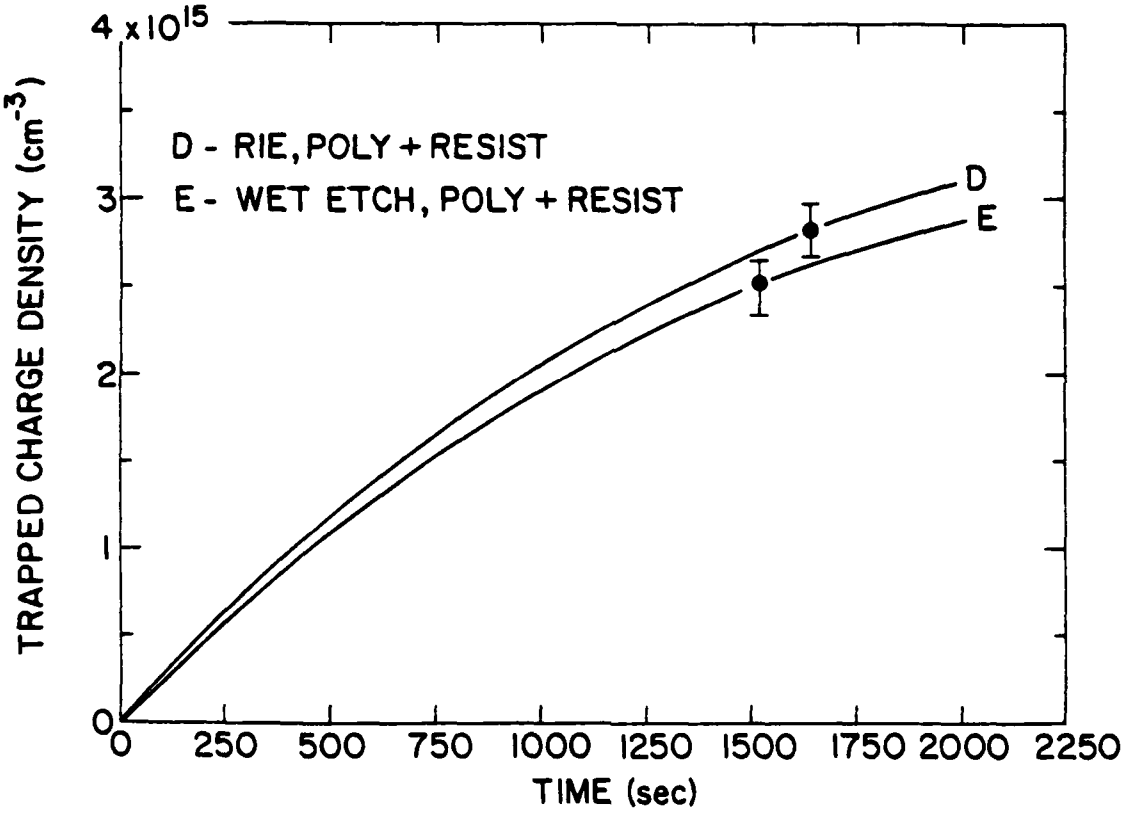
E NO RIE
B RIE, Al
A
E
B
0
250
750
1250
1750
2250
TIME (sec)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3
2
1
0
TRAPPED CHARGE DENSITY (cm^-3)
D - RIE, POLY + RESIST
E - WET ETCH, POLY + RESIST
D
E
0
250
500
750
1000
1250
1500
1750
2000
2250
TIME (sec)

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Capture and Release of Electrons on Na^+-Related Trapping Sites in the SiO_2 Layer of MOS Structures at Temperatures Between 77°K and 296°K*

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Typed by Stella B. Havreluk (3277)

Abstract: Electron trapping and detrapping mechanisms on Na^+ ions near the Si-SiO_2 interface of MOS structures and the location of these captured electrons were studied as a function of temperature from 77°K to 296°K. Capacitance -voltage (C-V) and photocurrent-voltage (photo I-V) techniques have been used to directly show that the charge neutralization on the Na^+ ions takes place spatially in the immediate vicinity of the ions near the Si-SiO_2 interface. Experiments reported here indicated that Na^+ ions neutralized at 77°K by electron capture do not become charged again even under negative voltage stressing conditions if the sample is heated to 296°K. This applies if the initial areal density of Na^+ ions near the Si-SiO_2 interface is less than $\approx 3.7 \times 10^{12}$ cm^{-2}. For densities greater than $\approx 3.7 \times 10^{12}$ cm^{-2}, Na^+ motion back to the Al-SiO_2 interface under negative voltage bias can be observed due to incomplete neutralization. Other experiments have shown that the electron capture process on Na^+ related sites (with capture cross sections of 2×10^{-19} cm^2 and 5×10^{-20} cm^2) decreases with increasing temperature as the MOS is warmed from 77°K and stops at $\approx$ 158°K. However, electron capture resumes again when the sample is cooled. This phenomenon appears to depend somewhat on local electric fields near the Si-SiO_2 interface and is reversed (trapping increases with temperature) for large initial Na^+ ion densities ($\approx 6.1 \times 10^{12}$ cm^{-2}). Several models are discussed which are consistent with the overall picture for the neutralization process.

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I. Introduction

Previously, it has been shown that Na^+ ions drifted towards the $Si–SiO_2$ interface of an MOS structure can be completely neutralized, as inferred from capacitance-voltage (C-V) measurements, by electronic avalanche injection at 77°K for ion concentrations of less than approximately 3.7×10^{12} cm^{-2} [1]. In these C-V measurements, flat-band voltage shifts associated with the electron trapping in the SiO_2 layer were studied as a function of the initial flat-band voltage shifts due to the presence of Na^+ ions in the SiO_2. The dominant electron capture cross sections associated with the Na^+ related trapping sites were 2×10^{-15}, 2×10^{-19}, and 5×10^{-20} cm^2 with most of the trapped charge associated with the latter two cross sections [1]. In a later publication, it was shown for the temperature (20-40°C) and bias (2-4.5 MV/cm) stressing conditions of these experiments that the drifted Na^+ ions lie within 50 Å of the $Si–SiO_2$ interface [2]. In this article, the results of another series of experiments are reported which were designed to provide further information about the location of the trapped electrons which neutralize the Na^+ ions, an upper limit for the number of ions that can be neutralized, the thermal release energy for trapped electrons on the Na^+ related sites, and the temperature dependence of these capture cross sections. Finally, all the experimental data will be pulled together and discussed in terms of several possible physical models which are consistent with the overall picture.

II. Experimental

A. Sample Preparation

The metal-oxide-semiconductor (MOS) capacitors used in this study were similar to those used in previous studies [1,2]. A 500 Å thick "dry" thermal oxide was grown on <100> orientation, 0.1–0.2 Ωcm p-type Si. NaCl was then evaporated onto the top surface of the oxide giving a level of $\geq 10^{13}$ Na^+ ions/cm^2 [1,2]. Next, either thick (2000 Å) or thin (135 Å) circular Al electrodes with an area of .005 cm^2 were evaporated to form an

MOS capacitor. Finally, a post-metallization forming gas anneal was performed to reduce $Si–SiO_2$ surface states. The samples with the thin Al electrodes were used in the photocurrent-voltage (photo I-V) measurements described in later sections.

B. Apparatus

Several experimental sets of apparatus described in previous publications were used in combination in this study. Avalanche injection [3-6], photocurrent-voltage (photo I-V) [7-9], capacitance-voltage (C-V) [10,11], flat-band voltage tracking [5,6], and low temperature apparatus [2] were all used. Na^+ ions were drifted at room temperature (20-30°C) under average applied electric fields of 2-4 MV/cm for either gate voltage polarity and quenched to liquid nitrogen temperature (77°K) under positive or zero gate voltage bias [2]. To vary the sample temperature between 77°K and room temperature an Air Products Heli-tran low temperature dewar was used [2]. Flat-band voltages were measured at selected time intervals using automated tracking circuits previously described [5,6]. Electronic and ionic currents were measured using a Keithley 616 digital electrometer. Average avalanche injection current densities from the Si substrate produced by 500 kHz square wave voltage pulses were varied from 10^{-8} to 10^{-3} A/cm^2 [1]. The current densities were kept constant by automatically adjusting the gate voltage to keep the electric field in the SiO_2 near the injecting interface ($Si–SiO_2$) constant [5,6]. Photo I-V measurements were performed in conjunction with 1 MHz C-V measurements using an automated set-up described previously [9]. The internal photoemission currents, on which the photo I-V technique is based [8,12,13], were injected from the $Al–SiO_2$ ($Si–SiO_2$) interface for negative (positive) gate polarity with 4.5 (5) eV light to sense the location and amount of the Na^+ ions and/or trapped electrons. All avalanche injections and photo I-V measurements were done at 77°K. Data reported here were reproducible from sample to sample and from samples fabricated months apart.

III. Trapped Electron Location

A series of experiments were performed using a combination of the photo I-V [2,8,9,13,14-16] and C-V techniques [10,11] to spatially probe the Na^+ neutralization process at 77°K by electron capture. These techniques are described in detail in the literature and will not be discussed here. Figure 1 shows photo I-V data for positive gate bias (Si injecting) at the following progressive stages of the experimental sequence:

A - no Na^+ ions at Si–SiO_2 interface at 77°K.

B - 3.1×10^{12} Na^+ ions/cm^2 at Si–SiO_2 interface at 77°K.

C - After electronic avalanche injection at 77°K under conditions required to neutralize or compensate the 3.1×10^{12} Na^+ ions/cm^2 at the Si–SiO_2 interface.

D - After warming to room temperature (following C) under a bias of $V_g = -15$ V and then quenching to 77°K.

The data in Fig. 1 can be interpreted in the following manner:

1. The distortion between curves A and B is due to the presence of Na^+ ions within at least 50 Å of the Si–SiO_2 interface [2,13,14,17]. The presence of the Na^+ ions near this interface gives the enhancement in photocurrent and increase in splitting between curves A and B with increasing positive gate voltage bias [2,13,14,17]. The interpretation and implication of this data has been discussed at length in a previous publication [2].

2. During electron avalanche injection, it has been reported previously from C-V measurements that a one to one relationship between electron trapping and Na^+ at the Si–SiO_2 interface is seen after correction for the normal back-

ground trapping of the oxide layer itself at 77°K [1]. Figure 1 shows directly that the enhanced trapping due to the Na^+ ions within 50 Å of the $Si-SiO_2$ interface is due to electron trapping spatially within this same region. This is deduced from the parallel nature of curve C (after avalanche charging) with respect to curve A ($[Na^+]=0$). The distortion present in curve B ($[Na^+]=3.1 \times 10^{12}$ ions/cm^2) as compared to curve A due to the positive charge of the Na^+ ions has been removed by a neutralization of the Na^+ ions by trapped electrons in this same spatial region. The parallel voltage shift between curves A and C is due to bulk oxide background trapping at 77°K [1,18-20]. A similar parallel voltage shift between a control sample with $[Na^+]=0$ before and after charging under avalanche injection conditions similar to those in Fig. 1 was also seen which supports the above arguments for Na^+ neutralization.

3. Curve D (sample warmed to room temperature under $V_g=-15$ V and then quenched to 77°K) shows that some of the normally present, bulk trapped oxide charge has been removed. However, no trapped electrons have been removed from on or near the Na^+ ions located within 50 Å of the $Si-SiO_2$ interface. On warming to room temperature, the flat-band voltage and d.c. dark currents were monitored. Flat-band voltage shifts yielded results similar to Fig. 2 and Fig. 3 implying no Na^+ motion under $V_g=-15$ V bias from the $Si-SiO_2$ interface back to the $Al-SiO_2$ were observed. Also the d.c. dark currents indicated no motion of Na^+ back to the Al electrode. These latter two points will be discussed in detail in the next section (IV - Detrapping). The photo I-V for negative gate voltage bias (Al-injecting) again showed the normal negative charging of the background oxide traps [18]. However as described in a previous publication [2], there was essentially little effect on these photo I-V characteristics caused by moving Na^+ ions from a deposited

NaCl layer very near the Al–SiO_2 interface to the Si–SiO_2 interface. Therefore, the neutralization of Na^+ at the Si–SiO_2 was not sensed by the Al–SiO_2 photo I-V characteristics which are more sensitive to changes in the internal electric fields caused by charging or discharging of traps nearer to this interface.

IV. Detrapping

In the next series of experiments, samples with various amounts of Na^+ drifted to the Si–SiO_2 interface at room temperature and neutralized at 77°K using avalanche injection of electrons from the Si substrate were warmed to room temperature (296°K) under a negative gate voltage bias of −15 V. This bias would pull Na^+ ions back to the Al–SiO_2 interface if trapped electrons were thermally released and/or if not all the Na^+ ions were neutralized. During the heat-up, flat-band voltage (V_{FB}) and the current in the external circuit (I_{ext}) were measured.

Typical data during warm-up to room temperature for V_{FB} as a as a function of time under a gate bias of −15 V are shown in Figs. 2-4 for difference initial Na^+ concentrations. All samples in Figs. 2-4 were avalanched at 1×10^{-3} A/cm^2 until the flat-band voltage was changing by less than 25 μV/sec prior to warm-up [1]. In Fig. 2 where there are no Na^+ ions purposely near the Si–SiO_2 interface and in Fig. 3 where all 1.7×10^{12} Na^+ ions/cm^2 near the Si–SiO_2 interface were neutralized [1], negative charge (corresponding to a flat-band voltage shift of $\simeq -3$ to −4 V) is observed to be thermally released between 200°K and 296°K. This negative charge is released from shallow traps in the <u>bulk</u> of the SiO_2 layers as verified by comparing changes in the flat-band voltage and photo I-V voltage shifts [2,13,14,17]. A control sample which had no Na^+ near the Si–SiO_2 interface and which had not been charged by avalanche injection showed less than a +.2 V flat-band shift on heating to room temperature. Also a small net current of $\approx$ 1-3 $\times 10^{-12}$ A was observed in the

direction of electrons flowing out of the Si substrate into the electrometer after correction for a small constant background current associated with the heating of the sample to room temperature. The rate of change of the flat-band voltage $d(\Delta V_{FB})/dt$ is also very similar in Figs. 2 and 3 when thermal detrapping was observed. If electrons were being thermally released from Na^+ related sites in Fig. 3, a sudden increase in current and sudden change in the flat-band voltage should have been observed near room temperature when mobile Na^+ drifted back to the Al–SiO_2 interface. This was seen on a control with unneutralized Na^+ near the Si–SiO_2 interface. It was concluded from these results that once neutralized at 77°K by trapping electrons, Na^+ related sites stay neutral up to 296°K. The electrons discharged in Figs. 2 and 3 therefore, are from background oxide traps [1,18-20].

Figure 4 shows V_{FB} as a function of time under a −15 V gate bias during warm-up from 77°K to 296°K on a sample which has 6.1×10^{12} Na^+ ions/cm^2 drifted to the Si–SiO_2 interface at room temperature, was quenched to 77°K, and then avalanched at 1×10^{-3} A/cm^2 until the rate of change of the flat-band voltage due to electron capture was $\leq$ 25 μV/sec. This Fig. 4 shows a dramatic increase of the flat-band voltage near room temperature due to Na^+ motion from the Si–SiO_2 interface back to the Al–SiO_2 interface. Ionic currents measured when 296°K was reached (see point 4 in Fig. 4) were $6\text{-}7 \times 10^{-12}$ A in the direction of positive charge flow towards the metal gate electrode. Calculations of C_{ox} $d(\Delta V_{FB})/dt$ at this point yielded results of the same magnitude ($6\text{-}7 \times 10^{-12}$ A). The measured ionic current should be equivalent to C_{ox} $d(\Delta V_{FB})/dt$ if the shift in the flat-band voltage is mostly due to Na^+ motion back to the Al–SiO_2 interface and not due to release of trapped electrons. Calculations of C_{ox} $d(\Delta V_{FB})/dt$ at 296°K in Figs. 2 (no Na^+) and 3 (complete Na^+ neutralization) which is due to trapped electron release, yielded values $\lesssim 1 \times 10^{-12}$ A. However, it is reasonable that trapped electron release due to background oxide charging [1] is also occurring in Fig. 4 (although it is not as apparent as in Figs. 2-3) based on the observation that V_{FB} is approaching a steady state value of $\approx$ +3 V in all three cases.

The Na^+ observed to drift in Fig. 4 is due to incomplete neutralization of the ions near the Si–SiO_2 interface for large densities. Data in a previous publication (see Fig. 1 of reference 1) shows one trapped electron associated with each neutralized Na^+ ion for densities up to $\approx 3.7 \times 10^{12}$ Na^+ ions/cm^2 after avalanche injection at 77°K. However, in this study by extending the data to larger Na^+ densities, we have observed that the neutralization stops for ions densities approximately in excess of this level. Also, ion drift similar to that in Fig. 4 and the corresponding ionic currents were observed for densities $< 3.7 \times 10^{12}$ Na^+ ions/cm^2 when the avalanche current was terminated prematurely before complete neutralization occurred. The experiments described in this section lead to two important conclusions:

(a.) Electron trapping on Na^+ related sites at 77°K will only occur for $[Na^+] \lesssim 3.7 \times 10^{12}$ ions/cm^2. Any Na^+ ions approximately in excess of this density will not capture electrons under the avalanche injection conditions used here. This observation strengthens a previous speculation that electron capture on Na^+ related sites was dependent on their location and interaction with the surrounding lattice [1].

(b.) Once captured on a Na^+ related site an electron will not be released thermally at temperatures between 77°K and room temperature. However, at temperatures above 77°K the neutralization process via electron capture can be slowed down or stopped as will be discussed next.

V. Trapping Rate

The trapping rate for electron capture on Na^+ related sites was investigated by observing changes with temperature in the time rate of change of the flat-band voltage under avalanche conditions as indicated in Fig. 5. In this figure, a sample with initially 3.7×10^{12} Na^+ ions/cm^2 was avalanched at a current level of 1×10^{-3} A/cm^2 until the Na^+ related

traps with cross sections $\leq 2 \times 10^{-19}$ cm^2 (which is the majority of these traps) were being filled [1]. As seen by increasing the temperature from 77°K to 158°K, the trapping stops abruptly. On cooling to 77°K the trapping starts again at the same rate it had before the warm-up. Again on heating to 158°K, the trapping stops abruptly as shown in Fig. 5. At temperature between 77°K and 158°K, the trapping rate decreases with increasing temperature.

Experimentally, several possible mechanisms to explain Fig. 5 were ruled out and each will be discussed separately. These mechanisms were positive charge compensation [18], impact ionization of trapped electrons [21-23], field ionization or field assisted thermal detrapping, and Na^+ drift from the Al–SiO_2 interface towards the Si–SiO_2 interface.

Positive charge compensation at the Si–SiO_2 interface while negative trapping still proceeds in the bulk of the SiO_2 layer which has been observed at room temperature but not at 77°K at these avalanche injection current densities [18] is ruled out by the data of Fig. 5. If positive charge compensation is occurring on heating to 158°K, then the trapping rate after a return to 77°K in Fig. 5 should be different (possibly accelerated due to the presence and/or annihilation of the positive charge) than before warm-up to 158°K. This is not the case experimentally as seen from the data of Fig. 5.

Impact ionization of trapped electrons (especially next to the Si–SiO_2 interface) by incoming "hot" conduction band electrons [21-23] can not explain Fig. 5. This process if operative would cause the apparent net trapping rate to decrease with decreasing temperature because at lower temperatures the incoming electrons would be hotter due to less phonon scattering in both the Si and SiO_2.

Field ionization or field assisted thermal detrapping mechanisms were investigated and ruled out as a possible explanation for the data shown in Fig. 5. After avalanche charging of the SiO_2 layer to electronic charge levels equivalent to those shown in Fig. 5 for similar initial

Na^+ densities, the avalanche current was shut off and the sample stressed at constant voltages comparable to those across the oxide during avalanche injection. Periodically, the flat-band voltage was measured using the automatic tracking set-up described previously to ascertain the amount of trapped electrons removed from the oxide layer. White light from a high intensity tungsten lamp was used to insure rapid formation of the inversion layer and therefore negligible voltage drop across the Si for all positive gate biases [1]. Although these experiments showed a very small amount of negative charge being removed at a very slow rate, this could not account for the dramatic effects seen in Fig. 5. Also, the rate of charge removal with stressing voltage was not a strong function of temperature contrary to the observations of Fig. 5.

Na^+ drift from the Al–SiO_2 interface towards the Si–SiO_2 interface during avalanche injection was investigated as a possible explanation of the data of Fig. 5. However, no Na^+ ions were observed to drift at temperatures $< 170°K$ under constant field conditions comparable to those used during avalanche injection.

Having ruled out all of the obvious explanations not related to capture, the temperature dependence seen in Fig. 5 must be explained by the details of the electron capture process itself. This will be discussed in detail in the next section and several possible physical models proposed for the experimental observations.

However, the phenomenon displayed in Fig. 5 appear to be also dependent on local electric fields in the oxide which can be varied by changing the initial $[Na^+]$ near the Si–SiO_2 interface. In fact for $[Na^+] \approx 6.1 \times 10^{12}$ ions/cm^2, the rate of change of the flat-band voltage with time is enhanced at 158°K instead of reduced as compared to 77°K. These same trends were also seen when the avalanche current level was reduced to 1.5×10^{-4} A/cm^2; however, the trapping did stop at somewhat higher levels of negative trapped charge.

With no intentional Na^+ ions ($[Na^+]=0$) near the Si–SiO_2 interface, the trapping rate abruptly reversed on warming to 158°K and trapped electrons appeared to be detrapped for sites with similar cross sections ($\leq 2 \times 10^{-19}$ cm^2 [1]) as those observed for Na^+ neutralization. On cooling back to 77°K, electron trapping again started, only at an enhanced rate. Here, trapped electrons in the SiO_2 film are being discharged due to the higher local electric fields caused by a larger net amount of negative trapped charge for the same avalanche injection conditions used in probing the same cross section traps when Na^+ ions are present near the Si–SiO_2 interface.

Temperature dependence studies of the capture rate using avalanche injection were difficult at temperatures below 77°K due to carrier freeze out in the bulk of the Si substrate [24] and were not attempted. Hole freeze out on acceptor sites would manifest itself in the inability to form depletion charge (ionized acceptors), and therefore the high field region necessary for avalanche breakdown in the pulsing times used ($\approx 1 \times 10^{-6}$ sec).

VI. Discussion

A. *Coulombic Capture*

One possible explanation, and perhaps the most reasonable, for electron capture on Na^+ related trapping sites based on experimental results from this study and previous publications [1,2] is summarized in Fig. 6. Initially after drift at room temperature under positive voltage bias, the Na^+ ions are located very near the Si–SiO_2 interface [2]. From work function arguments, it would be expected that the Na^+ levels are energetically very shallow with respect to the SiO_2 conduction band as shown in Fig. 6a [25]. However, because the Na^+ is very close to the Si–SiO_2 interface, it should be somewhat influenced by the nature of the interface and the lattice surrounding the Na^+ ions; that is, stoichiometry variations, image forces, etc.

Although the Na^+ ions do not trap electrons at room temperature, they can be completely neutralized for densities less than $\approx 3.7 \times 10^{12}$ ions/cm^2 at 77°K with capture cross sections of 2×10^{-15} cm^2, 2×10^{-19} cm^2, and 5×10^{-20} cm^2 [1]. Most of the electron trapping on these sites is associated with the latter two small cross sections deduced from data fitting of the change in flat-band voltage with time under constant avalanche injection current densities [1]. No neutralization of Na^+ is seen for ions in excess of $\approx 3.7 \times 10^{12}$ cm^{-2} under the conditions for the experiments described here. These observations support previous speculations that the Na^+ location [1] in the vicinity of the Si–SiO_2 interface influences the trapping process perhaps by giving different energy levels for different Na^+ sites as shown in Fig. 6a. Na^+ ions at the Si–SiO_2 interface which may or may not be energetically shallow with respect to the SiO_2 conduction band would be expected to be very difficult to neutralize because of back-tunneling of partially bound electrons to the empty Si conduction band states.

If the Na^+ sites are energetically shallow, attractive coulombic traps, the low capture cross section values should increase as the temperature is lowered [26-30] which is observed experimentally. Ultimately, at very low temperatures (probably < 10°K), a value of 10^{-12}-10^{-13} cm^2 for low applied fields [14,22,26,33-35] indicative of a coulombic attractive capture cross section should be observed. The shallow energy level argument for Na^+ traps is supported by observations that positively trapped holes near the Si–SiO_2 interface [14,17,30-32] which are energetically deep at least with respect to the SiO_2 valence band [36] do behave like attractive coulombic sites for electrons at room temperature [14,17,37]. The interfacial sites which trap holes and those which hold the Na^+ ions are probably not the same.

Once an electron is captured by an Na^+ related trapping site, it is observed experimentally to be located spatially in the vicinity of the Na^+ ions and is stable against thermal detrapping at least up to room temperature. This implies that once an Na^+ ion is neutralized by electron capture, the energy level must move down with respect to the SiO_2 conduction

band as shown in Fig. 6b. The energy level should be deeper than 3-4 eV to prevent electron back-tunneling to the Si substrate; that is, the captured electron must "see" filled Si valence band states, or possibly the Si forbidden band gap for neutralized ions far enough away from the interface so that they can not communicate thermally with the Si energy bands.

The phenomenon of an energy level becoming energetically "deeper" with respect to the SiO_2 conduction band after electron capture has been reported by Ning for some of the background native oxide trapping occurring at 77°K [20]. This process could be irreversible and involve a chemical reaction similar to what Nicollian et al. have suggested for electron capture at room temperature on H_2O related sites in SiO_2 in which atomic hydrogen, diffusing out of the SiO_2 layer, has been detected after electron capture by the H_2O related sites [38].

The oxide fields near the Si–SiO_2 interface used in these experiments ($\gtrsim$ 1 MV/cm) are large enough to also greatly enhance the probability of thermal re-emission of a carrier by barrier lowering, particularly if the trapping site is $\lesssim$ 1 eV deep from the bottom of the SiO_2 conduction band. For example, with fields in the range of 1 MV/cm to 6 MV/cm, the barrier lowering $\Delta\Phi$ is .52 eV to 1.26 eV. This is determined using the relationship $\Delta\Phi = 2\sqrt{q\mathcal{E}/(4\pi\varepsilon_i)}$ [11] where q is the magnitude of charge on an electron, $\mathcal{E}$ is the electric field, and ε_i is the high frequency permittivity of SiO_2 ($\varepsilon_i \approx 2.16 \times 8.86 \times 10^{-14}$ F/cm). This barrier lowering can be further influenced by the interaction of the potentials of neighboring ions. For example, Na^+ ions near the Si–SiO_2 interface with densities in the range from 1×10^{12} to 6.1×10^{12} cm^{-2} would have average separations from 41 Å to 100 Å. This would lead to and addition component to the barrier lowering of as much as .3 eV at 77°K for the largest density used in this study [33]. Also, interaction of the potentials of neighboring Na^+ ions could also decrease the electron capture rate for some of the ions which experience the strongest interaction, at least until the neighboring ions are neutralized.

The influence of Na^+ clumping at the Si–SiO_2 interface should not affect the energy levels greatly. For the Na^+ densities, deposition techniques, and drifting conditions used here, clumping of Na^+ ions is not expected to occur [39].

B. Repulsive Coulombic and Neutral Capture

Another possible explanation exists for the very low magnitude (2×10^{-19} and 5×10^{-20} cm^2 [1] of the capture cross sections associated with most of the Na^+ related trapping sites. This explanation requires a repulsive potential well for the Na^+ sites even though the ions are positively charged. This repulsive potential could come about in several ways. A dipolar type of trapping center formed by an Na^+ ion very near the Si–SiO_2 interface, and the electron it attracts to the Si surface from the bulk of the Si (image charge) is one type of repulsive trap. This type of repulsive center would have a directional dependence [40]. Incoming electrons from the Si substrate would "see" a repulsive potential caused by the image charge, while electrons moving from the Al electrode towards the Si substrate would "see" an attractive potential with, however, a limited range due to the dipolar nature of the center. Similarly, a repulsive trap could be formed in a polar material like SiO_2 due to the attraction of a portion of the electron clouds surrounding neighboring atoms by an Na^+ ion. This type of center would probably not have any strong directional dependence, and it would be sensitive to the local lattice environment. Figure 7 shows the potential energy distributions for the various types of capture centers discussed with a neutral trapping center (Fig. 7b) included for completeness [26].

Neutral trapping centers are expected to have capture cross sections with a magnitude of 10^{-15}–10^{-16} cm^2. This value is deduced from assuming that the capture cross section for a neutral center is given approximately by πr_c^2 where r_c is of atomic dimensions; that is $r_c \approx 10^{-18}$ cm [28]. Those Na^+ related trapping sites with a low density are observed to

have a larger capture cross section of 2×10^{-15} cm^2 which is in the range of that expected for neutral trapping centers.

The temperature dependence of a repulsive trapping site could also be explained by the data of Fig. 5. Electrons entering the oxide from the Si at 77°K are "hotter" than those entering at 158°K and are less likely to scatter off phonons in the oxide and lose energy (see section IV-C). Those "hot" electrons are more likely to surmount or tunnel into the repulsive potential as depicted in Fig. 7c. Therefore, the capture cross section would decrease as temperature is increased, consistent with the data presented here.

The temperature dependence expected for capture into neutral trapping sites is not consistent with the data of Fig. 5. The capture cross section for a neutral trap would increase with increasing temperature [30,41]. For neutral capture, an increase in lattice vibrations (phonons) with temperature would allow a trapping level to energetically cross into the SiO_2 conduction band, capture an electron, and then move to a deeper position in the SiO_2 bandgap relaxing by multiphonon emission [30,41]. This type of behavior has been observed for energetically deep impurity levels in semiconductors like GaAs or GaP [41].

C. Electron Heating

The temperature dependence of the capture process can be divided into the heating and thermalization of the incoming electrons and the temperature dependence of the capture cross section of the traps. The latter point has been discussed in section VI-A. The former point will be discussed here. It depends on the energy distribution of hot electrons entering from the Si, the proximity of the Na^+ related trapping sites to the $Si–SiO_2$ interface, and thermalization of these hot electrons in the SiO_2 layer. Avalanche injected electrons at 77°K are somewhat hotter than those at 158°K because of less phonon scattering through the Si space charge region [42,43]. However, the difference is not very large [42]. These "hot" electrons on entering the oxide would thermalize in the oxide by phonon scattering more

rapidly at 158°K than at 77°K. For Na^+ ions < 50 Å from the Si–SiO_2 interface [2], most of these entering electrons would not lose much energy as they transversed the Na^+ ion region if reasonable oxide phonon scattering lengths (10-60 Å [44-46]) are assumed. Clearly, if electron heating effects in the Si or SiO_2 layers are important for the conditions of the experiments described here, the trapping rate should increase with increasing lattice temperature. This is not observed for $[Na^+] \leq 3.7 \times 10^{12}$ cm^{-2} (see section V) and is consistent with the arguments presented in this section.

D. Local Electric Fields

The increase in the electron capture rate at 158°K over that at 77°K for initial Na^+ concentrations of $> 3.7 \times 10^{12}$ ions/cm^2 is a puzzling result. At 77°K, the trapping rate is not very sensitive to the Na^+ ion concentration. This observation was also reported before [1]. One possible explanation would be due to a decrease of the magnitude of the local electric field near the leading edge of the Na^+ distribution (away from the Si–SiO_2 interface) with increasing $[Na^+]$ (the field near the injecting interface is always kept constant for a given avalanche current). Why this mechanism should be operative at 158°K and not at 77°K is also difficult to explain. Perhaps, the lower energy of the incoming electrons and their increased scattering at 158°K couple with the local electric fields to enhance their capture probability. Incoming higher energy electrons with less oxide scattering at 77°K probably would be less sensitive to changes in local electric fields.

VI. Conclusions

The results presented here and in previous publications [1,2] should be considered together with recent publications by Fowler and Hartstein who have studied the effect on inversion layer electrons in metal-oxide-semiconductor field-effect-transistors (MOSFETs) of Na^+ ions drifted to near the Si–SiO_2 interface [47-49]. Their Na^+ deposition, sample

fabrication, and drifting techniques are similar to ours. Fowler and Hartstein have come to the following conclusions from their work:

1.) Most of the Na^+ are energetically deep (about 3 to 4 eV from the bottom of the SiO_2 conduction band edge and behave mostly as donor-like interface states (that is, positively charged when not filled by electrons) communicating with the Si bands [47] and partially ($\approx$ 20% of the Na^+ drifted) as oxide charge with which inversion layer electrons can form bound states leading to an impurity band $\approx$ 20-30 meV below the bottom of the Si conduction band [49]. These results were determined from measuring and comparing the conductance and the low frequency capacitance of their MOSFETs at temperatures from 77°K to 4°K [47-49].

2.) The fraction of Na^+ which act as oxide charge forming a Si impurity band are $\lesssim$ 4 Å *from the Si–SiO_2 interface as deduced from matching their experimental* results to the theory for the binding energy [49] and for the effects of ionic scattering on electron mobility in the channel of the MOSFET [50,51].

However, our results from reference 2 suggest that most of the Na^+ ions are $\gtrsim$ 4 Å away from the Si–SiO_2 interface. In this publication and in a previous publication [2], photo I-V voltage shifts for positive gate voltages at electric fields near the Si–SiO_2 interface of 1.5–2 MV/cm are approximately equivalent to a high-frequency (1 MHz), small-signal flat-band voltage shifts. This implies that most of the Na^+ causing the photo I-V shift is $\gtrsim$ 4 Å from the Si–SiO_2 interface if a simple Schottky barrier lowering model is used [11]. Also, since the photo I-V technique is most sensitive to bulk SiO_2 charges distributed away from the Si–SiO_2 interface [2,8,13-15] while capacitance-voltage techniques which are used to measure the flat-band voltage are most sensitive to charges at the Si–SiO_2 interface [10,11], our results suggest that most of the Na^+ ions that are counted from flat-band voltage measurements behave like oxide charges and stay ionized regardless of the position of the Si Fermi

level with respect to the Si energy bands. In the photo I-V measurements, the 0.1-0.2 Ωcm p-type Si substrates used were biased into inversion (the Fermi level is near the bottom of the Si conduction band) so that all the surface states are filled with electrons, while for the flat-band voltage measurements most of the surface states are empty (the Fermi level is near the top of the Si valence band). However, at higher Na^+ levels ($\gtrsim 3 \times 10^{12}$ ions/cm^2), some deviations in the flat-band and photo I-V voltage shifts were observed (photo I-V voltage shifts were smaller) suggesting the possibility that part of the flat-band voltage shift was due to interface states in the upper part of the Si bandgap caused by the Na^+ ions or their presence. Another possible explanation for the observed deviations could be due to some of the Na^+ ions in the SiO_2 being very near the Si.–SiO_2 interface which were not detected with the photo I-V measurement due to the limited voltage range scanned [2,8,13-15]. These Na^+ ions could act as oxide charges and not exchange electrons with the Si bands, particularly if they are $\lesssim 3$ eV in depth from the bottom of the SiO_2 conduction band. This deviation of the flat-band voltage shift and photo I-V voltage shift for positive gate voltage bias is shown in Fig. 8. This deviation starts in the vicinity of $\approx 3 \times 10^{12}$ Na^+ ions/cm^2 as counted by the flat-band voltage measurements which we used in previous publications [1,2]. It is interesting to note that Na^+ in excess of $\approx 3.7 \times 10^{12}$ ions/cm^2 as counted by flat-band voltage measurements can not be neutralized (see section IV). These two observations suggest the possibility that the excess Na^+ ions that can not be neutralized are very near the Si–SiO_2 interface and lie energetically at most 4 eV deep with respect to the bottom of the SiO_2 conduction band. This means electrons can not stay on the Na^+ sites, but must either tunnel or be thermalized if within ≈ 3 eV or ≈ 4 eV of the bottom of the SiO_2 conduction band, respectively, to empty conduction band states in the Si near the interface.

Some of these differences between the two groups of measurements (Na^+ trapping and the inversion layer studies) might be resolved because of the different techniques used (conductance of the inversion layer electrons of the MOSFETs, high frequency capacitance at

1 MHz, low frequency capacitance, and photo I-V) sense different charged sites in the oxide and/or at the Si–SiO_2 interface.

The inversion layer conductance measurements look at both the oxide charges and filled interface states, since the Fermi level in the Si is near the bottom of the Si conduction band for these measurements on n-channel MOSFETs. Negatively charged interface states could compensate some of the positively charged Na^+ ions which could act as oxide charges. High frequency capacitance only looks at interface states which can follow the 1 MHz signal. If these are related to any fraction of the Na^+ ions, these ions would have to be very close to the Si–SiO_2 interface. The low frequency capacitance measurements of Fowler and Hartstein [47] look at fast and slow interface states. The slow states can be distributed further into the oxide and have slow response times in communicating with the Si bands. If the flat-band voltage position of the capacitance-voltage curves is used, the Fermi level is near the Si valence band and the measured voltage shifts look at the sum of oxide charges, unfilled interface states above the Fermi level position, and any interface states near the Fermi level which can follow the measuring frequency.

Our measurements, in particular the photo I-V results in Fig. 1 of reference 2 and those presented here in Fig. 1, are least sensitive to interface states associated with the Na^+ ions or caused by their presence possibly through lattice distortions as compared to the results of Fowler and Hartstein. The interface states that have been studied by Fowler and Hartstein could be related directly to such lattice distortions, rather that to states associated with just the Na^+ ions themselves, although Fowler and Hartstein do get a good fit of their experimental MOSFET electron mobilities to a scattering theory involving only Na^+ ions [48]. It is also interesting to note that Fowler and Hartstein also saw differences like that in Fig. 8 when they plotted flat-band voltage shifts as a function of threshold voltage shift of their MOSFETs, only this difference was much larger for a similar range of $[Na^+]$ counted from the

threshold voltage shift measurements [47]. Fowler and Hartstein never observed a range where the voltage shifts were equivalent like that shown in Fig. 8.

Simple work function arguments for sodium atoms in a vacuum suggest that the Na^+ levels are not more than 2 eV deep from the bottom of the SiO_2 conduction band edge [25]. This again seems contrary to the results of Fowler and Hartstein. However, interaction of the Na^+ ions with the SiO_2 lattice near the Si–SiO_2 interface and with electrons in the Si substrate might cause the sites to be energetically deeper with respect to the bottom of the SiO_2 conduction band and therefore communicate with the Si energy bands. Also, the presence of the Na^+ ions near the Si–SiO_2 interface could create interface states due to distortions in their lattice environment which they caused. This latter type of argument would allow the Na^+ ions to act as shallow trapping sites for electrons, but also produce interface states that could interact with the Si energy bands depending on the range of the lattice distortion resulting from the Na^+ ions. The exact energy position in the SiO_2 bandgap of the Na^+ ions is not crucial in explaining the data contained in this paper or references 1 and 2, and has been discussed at length in section V. There still seems to be a lack of a complete understanding of the exact nature of the Na^+ induced trapping sites, the Si–SiO_2 interface states, and Si impurity bands they cause. Hopefully, future experiments will increase our knowledge of this complex situation when Na^+ is drifted near the Si–SiO_2 interface.

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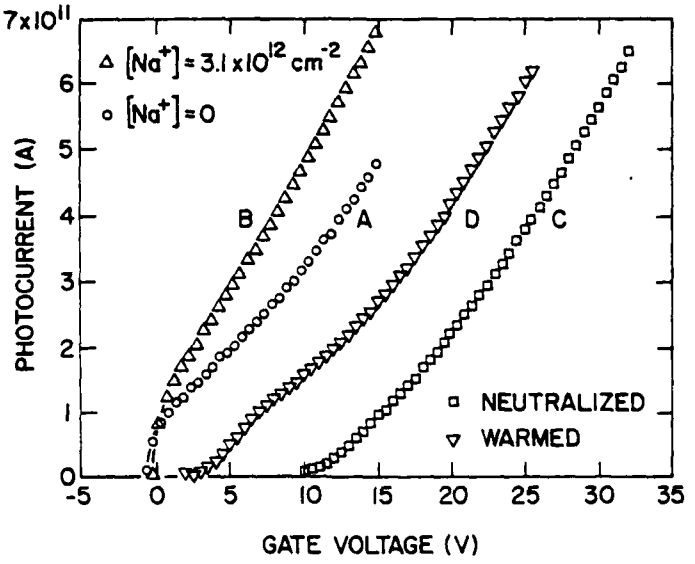

Figure 1. Photocurrent at 77°K as a function of positive gate voltage bias (Si-injecting) for 5 eV light. (A) - $[Na^+] = 0$ at the Si–SiO_2 interface. (B) - $[Na^+] = 3.1 \times 10^{12}$ cm^{-2} at the Si–SiO_2 interface after Na^+ ion drift at room temperature. (C) - Na^+ ions (3.1×10^{12} cm^{-2} from (B) neutralized by avalanche injection from the Si at 77°K. (D) - sample from (C) warmed to room temperature under −15 V gate bias then quenched back down to 77°K.

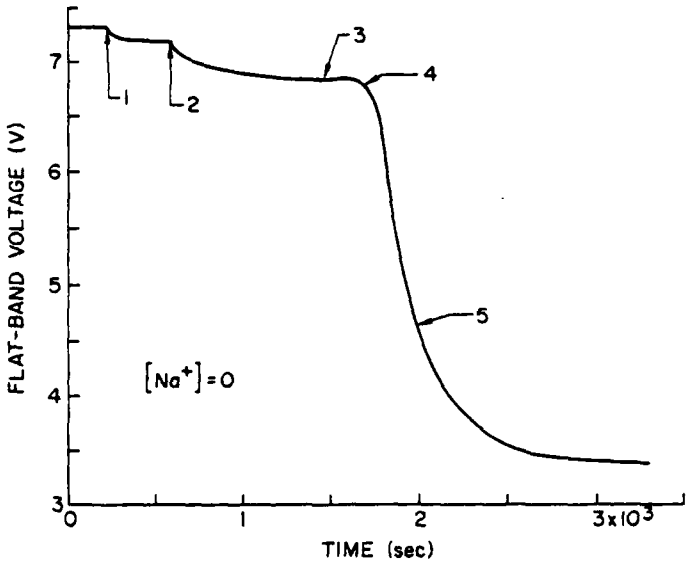

Figure 2. Flat-band voltage as a function of time for an MOS structure warmed from 77°K to 296°K. [Na^+] near Si–SiO_2 interface prior to avalanche injection and warm-up was ≈ 0 ions/cm^2. Avalanche current at 77°K was 1×10^{-3} A/cm^2 until a rate of change of the flat-band voltage of $\lesssim 25$ μV sec was reached. The sequence as indicated on this figure for the warm-up was (1) - the avalanche current was shut off and gate bias set at 0 V, (2) - a −15 V gate bias was applied, (3) - warm-up from 77°K to room temperature started, (4) - temperature of 200°K was reached, and (5) - temperature of 296°K (room temperature) was reached.

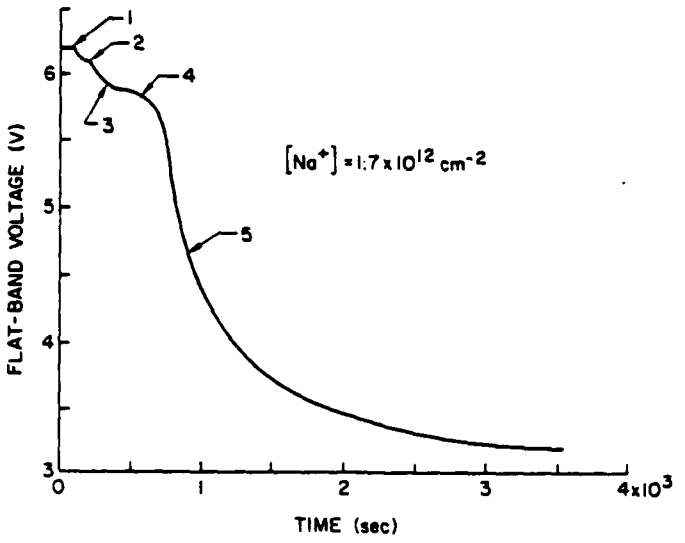

Figure 3. Flat-band voltage as a function of time for an MOS structure warmed from 77°K to 296°K. [Na^+] near Si–SiO_2 interface prior to avalanche injection and warm-up was 1.7 × 10^{12} ions/cm^2. Conditions for avalanche charging and warm-up are the same as in Fig. 1.

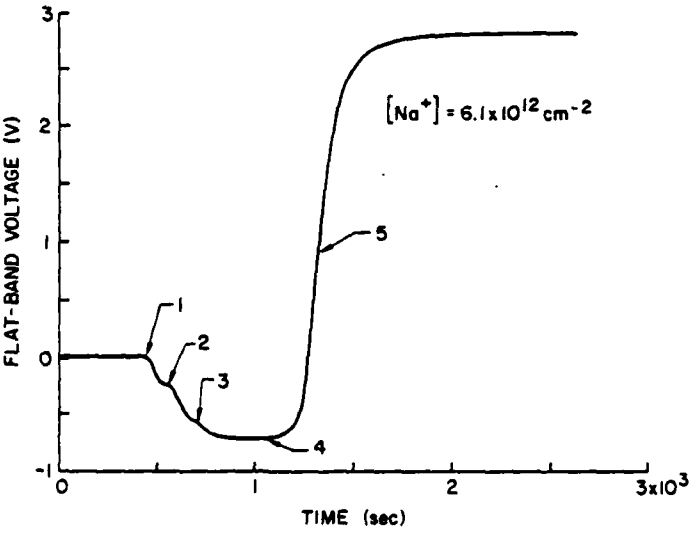

Figure 4. Flat-band voltage as a function of time for an MOS structure warmed from 77°K to 296°K. [Na^+] near Si–SiO_2 interface prior to avalanche injection and warm-up was 6.1 × 10^{12} ions/cm^2. Conditions for avalanche charging and warm-up are the same as in Fig. 1.

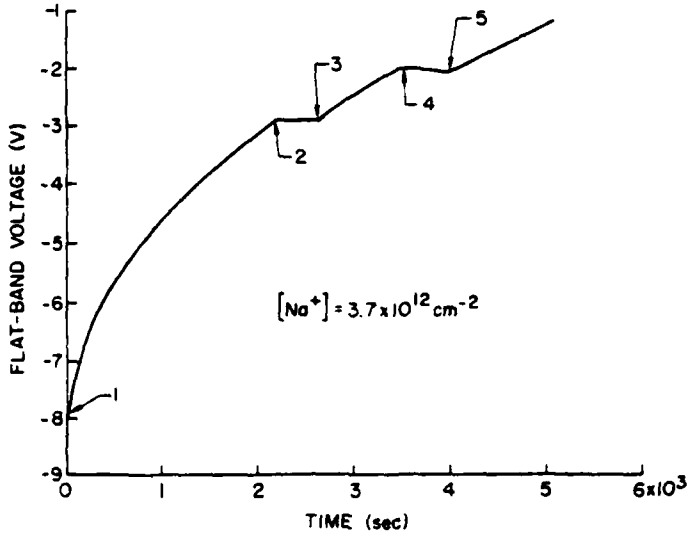

Figure 5. Flat-band voltage as a function of time as Na^+-related traps capture electrons under an avalanche injection condition of 1×10^{-3} A/cm^2. Initial [Na^+] prior to avalanche injection was 3.7×10^{12} ions/cm^2. The experimental sequence was (1) - 1×10^{-3} A/cm^2 at 77°K begun, (2) - sample warmed to 158°K, (3) - sample cooled to 77°K, (4) - sample again warmed to 158°K, and finally (5) - sample cooled back to 77°K.

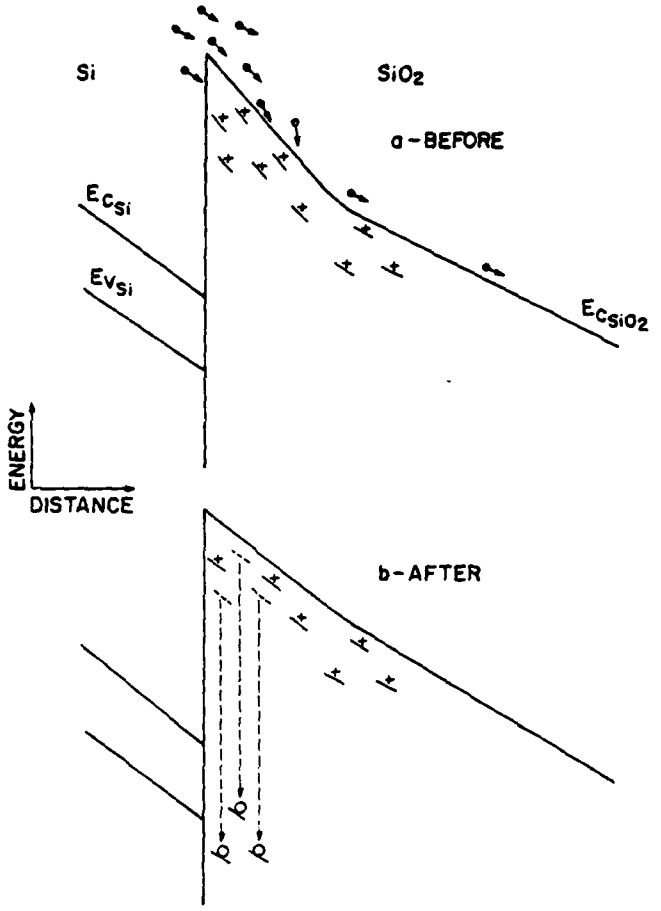

Figure 6. Energy band diagram of MOS structure under avalanche injection conditions with incoming "hot" electrons from the Si substrate crossing through the region near the Si–SiO_2 interface where there are related trapping sites (a) - schematic representation of energetically shallow Na^+ sites before electron capture (b) - schematic representation of energetically deep neutralized Na^+ sites after electron capture.

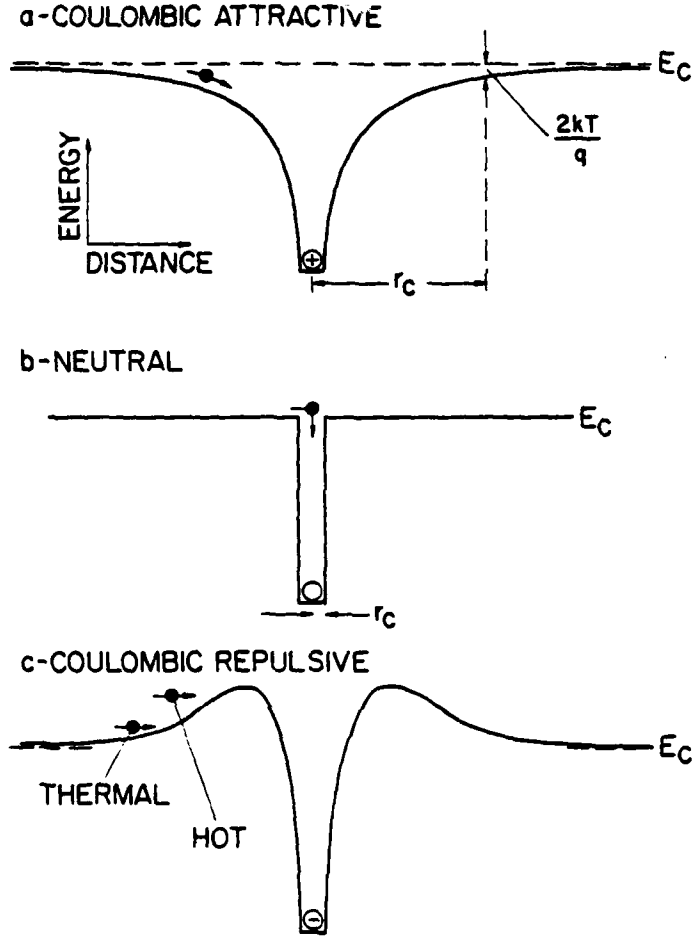

Figure 7. Schematic representation of potential energy distribution for (a) - coulombic attractive, (b) - neutral, and (c) - coulombic repulsive capture of SiO_2 conduction band electrons.

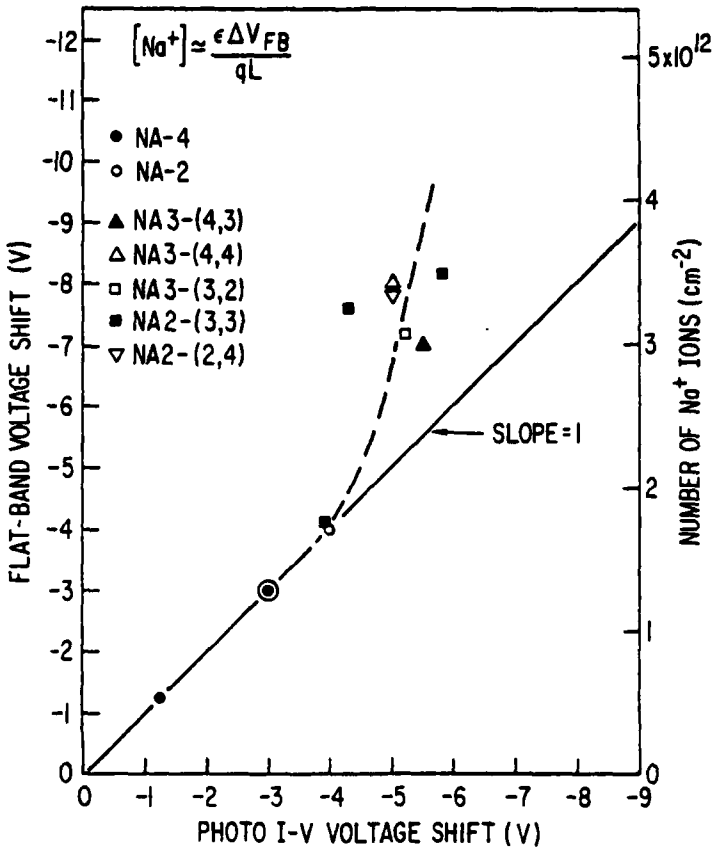

Figure 8. Flat-band voltage shift as a function of the photo I-V voltage shift for positive gate voltage for various numbers of Na^+ ions/cm^2, $[Na^+]$, as deduced from the flat-band voltage measurement where the Fermi level is near the top of the Si valence band for the .1 Ω-cm p-type Si substrate MOS structures used in these studies. $[Na^+] \approx (\epsilon\ \Delta V_{FB}) \div (qL)$ where ϵ is the low frequency permittivity of SiO_2, ΔV_{FB} is the flat-band voltage shift, q is the charge on an electron, and L is the SiO_2 thickness (≈ 500 Å). Samples Na-2 and Na-4 had rectangular gate areas as described in reference 2, while the NA2 and NA3 series of samples had circular gate areas of .013 cm^2 and .005 cm^2, respectively.

Automatic EAROM Cycling and Measuring System*

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Abstract

The Automatic EAROM Cycling and Measuring System (AECMS) is designed for the testing of single and dual electron injector structures in EAROM devices. The AECMS is used to measure shifts in the threshold voltage of the devices as a function of the number of write and erase cycles. It is capable of cycling devices to a maximum of 10^{12} times.

Introduction

This report describes the Automatic EAROM Cycling and Measuring System (AECMS) which is designed for the testing of dual electron injector structures (DEIS's) and single electron injector structures (SEIS's) incorporated into electrically-alterabale read-only-memory (EAROM) devices. The write or erase operation of the device is accomplished by applying a negative or positive square-wave voltage pulse respectively to a single control gate contact on 3 port devices. On 4 port DEIS EAROM's, only positive voltage pulses are used, and they are applied to either the control gate or the DEIS gate for write and erase operations, respectively, with the opposite gate grounded.

e Programmable Time Delay and Counter (PTDC) was designed primarily tc control the number of write/erase cycles applied to the device, delay 'ime between pulses, and the pulse period. These settings are controlled independently of each other by digital thumb-wheel switches on the front control panel. The PTDC module provides pulses to trigger two pulse generators, giving negative and positive pulses with the appropriate time delay and pulse period, and thus providing a continuous pulse train.

The read operation is accomplished by applying a voltage ramp to a device gate with the source of the FET at ground potential and with 100 mV on the drain. The threshold voltage is determined by measuring the source to drain current. After determining the initial threshold voltage,

the device is written and erased until a given preset number of cycles are reached. Then the threshold voltage window is determined by measuring the difference in the threshold voltages between the written and erased states of the device.

Experimental

The dual electron injector structure (DEIS) electrically-alterable read-only-memory (EAROM) is a non-volatile semiconductor memory device. The write and erase operations are based on high current injection into the SiO_2 from the Si-rich-SiO_2—SiO_2 interface [1-3]. This injection or removal of electrons, charges or discharges a floating poly-Si gate (storage layer). For the write operation with a three port structure [3], a negative voltage pulse is applied to the control gate to inject electrons into the floating poly-Si layer. While for the erase operation, a positive control gate voltage pulse is used to discharge this layer by removing electrons. The pulse width of the write or erase pulses can be on the order of milliseconds or microseconds, depending on the device configuration and voltage applied.

To minimize any movement while the device is under test, the sample is placed on a vacuum chuck. The probes are lowered onto the source, drain and gate contact pads for a 3-port devices (Fig.1). Also, 4-port devices can be tested by using an additional probe. For the case of 3-port devices, the write or erase operations are accomplished by applying a square-wave voltage pulse of negative or positive polarity, respectively, to a single control gate contact which has the DEIS stack underneath it. The square-wave voltage pulses are supplied by two Hewlett Packard Pulse Generators Model 214A. The Programmable Counter and Time Delay (PCTD) instrument was primarily designed to trigger the pulse generator to supply pulses as one continuous pulse train. This pulse cycle is not

available from a single pulse generator. This pulse cycle is achieved by selecting the appropriate time delay and pulse period. One output from the PCTD produces a reference pulse while the second output gives a pulse delayed beyond the first reference pulse by an amount determined from the front panel digit switches. The number of cycles can be preset to a given count, when the count is reached, the pulse train ends.

The written or erased state of the floating gate is determined by a specially designed threshold voltage detector. With 100 mV applied to the drain and with the source and substrate at ground potential, a voltage ramp with adjustable amplitude and ramp rate was used to supply the gate voltage V_g. The current between source and drain was measured with a Keithley Model 427 fast current amplifier. The voltage ramp and the amplifier are coupled through a comparator circuit which records the gate voltage at a preset value of the drain current I_d, and then resets the voltage ramp to zero. The drain current as a function of the gate voltage curves can be displayed on a Tektronix 7623 storage oscilloscope. The measurement time for determining the threshold voltage is approximately 2 milliseconds.

Operation

The operation of the Automatic EAROM Cycling and Measuring System (AECMS) is described in this section, and a system block diagram is shown in Figure 2. The operator manually sets the digital thumb-wheel switches on the front panel (Fig.3) to the appropriate cycling conditions: time delay, number of pulses, and pulse period. To ensure that no pulses appear at the output, it is necessary to toggle the clear/count switch before continuing. This operation eliminates any output pulses to the sample, before the actual cycling sequence occurs.

A 10MHz output clock is available from the programmable time delay card, Model-4145-2 by Evans Associates. This 10MHz frequency is applied to the input of a high-speed decade counter (SN7490) which divides the frequency by ten to provide a 1MHz square-wave output. The 1MHz clock is then applied to a divide-by-2 and a divide-by-5 counter to provide the appropriate pulse cycles for longer time periods. The time base circuit (MK5009P) is driven by the output pulses provided for by the counter, either directly, or divided by 2 or by 5, giving 1 MHz, 500 KHz or 200 KHz pulses, respectively. The MK5009P device then decodes the four control inputs, 2^0, 2^1, 2^2 and 2^3, to provide a minimum of divide-by-10^0, to a maximum of divide-by-10^8 counts, to give the output period desired. The control inputs are selected from the digital thumb-wheel switch on the front panel. The combination of two counters gives a maximum period of 500 seconds, to a minimum period of one microsecond. This will satisfy most requirements for cycling experiments. The divide-by-N counter and

time base circuits are shown in Appendix-A, Figure A-1.

The pulses provided for by the time base circuit, are applied to the count input of pulse counter circuit, which are shown in Appendix-A, Figures A-2 and A-3. The MK50395 is a six-decade synchronous up/down counter and display driver. The BCD register can be loaded digitally from the thumb-wheel switches on the front panel. The six-decade register is constantly comparing the state of the six-decade counter. When both the register and the counter have the same content, an "equal" signal is generated. This signal is applied to the input of an AND gate (CD4081B), and the output signal is applied to a Dual D-type flip-flop (CD4013). The "Q" output voltage level of the D-type flip flop controls the pulse train output from the NAND gate CD4011, which is applied to the trigger input of the programmable time delay card (Model 4145-2). The delay card has three outputs. One output produces a reference pulse having a fixed delay relative to the input pulse. The other output provides a pulse which is delayed beyond the reference pulse by a delay determined by the thumb-wheel switches on the front panel. The third output generates a gate pulse which is on for the period from reference pulse to the delay pulse. The circuits for the Programmable Time Delay module, Model4145-2 and the Model 4146 Digital Extender module are shown in Appendix-A, Figures A-4 and A-5.

The FET Ramp-Sample/Hold circuit is shown in Appendix-A, Figure A-6. To start the voltage ramp, a positive input pulse is generated by pushing the start button, or an external pulse can also be used. The

positive voltage pulse is applied to the base of transistor Q1, which is turned on, and puts the input of the SN7474 D-type flip-flop to a low state, and this sets the "Q" output voltage of the flip-flop to a low state, and the "Q not" (opposite of "Q") output voltage of the flip-flop to changes from a low state to high state. This high level is applied to the input of the AH0014D analog switch, allowing the switch to open. The short is removed from the integrating capacitor, which starts the voltage ramp . The output voltage from the ramp is applied to the gate of the device, and to the input of the HA2425 sample and hold i.c. The ramp voltage can be offset to start at a more negative or positive voltage, which forces the voltage ramp to increase either more negatively or positively, depending on the preceding offset voltage. This voltage is provied by adjusting the offset voltage applied to the inverting input of the op-amp, op-05.

The source to drain current from the FET device is applied to the input of the Keithley 427 Current Amplifier, which provides a negative output voltage proportional to the input current. The output voltage from the current amplifier is applied to the noninverting input of the LM311 voltage comparator, and a pre-set negative voltage is applied to the inverting input of the comparator. The current measured is increased with the voltage ramp until the the two input voltages to the comparator are equal, at which point the output switches to a low state. The low output from the comparator turns transistor Q2 off, which acts as an inverter. The clock input to the SN7474 D-type flip-flop changes from a low state to a high state and the "Q" output changes to the high state.

The SN7474 "Q" output triggers the HA2425 to sample, which is held in the hold mode, to hold the voltage ramp. This also triggers the DVM to take a voltage reading. The output voltage from the HA2425 is applied to the input of the Keithley 171 DVM which gives the voltage reading. The SN7474 also triggers a one shot SN74121(7). The one shot pulse is applied to the B input of the SN74121(3), which resets the ramp to zero. The ramp voltage and the output voltage from current amplifier, are displaved on the Tektronix 7623A oscilloscope. These voltage readings taken after the write or erase operations are used to determine the voltage window.

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DIAGRAM FOR SAMPLE MEASUREMENTS

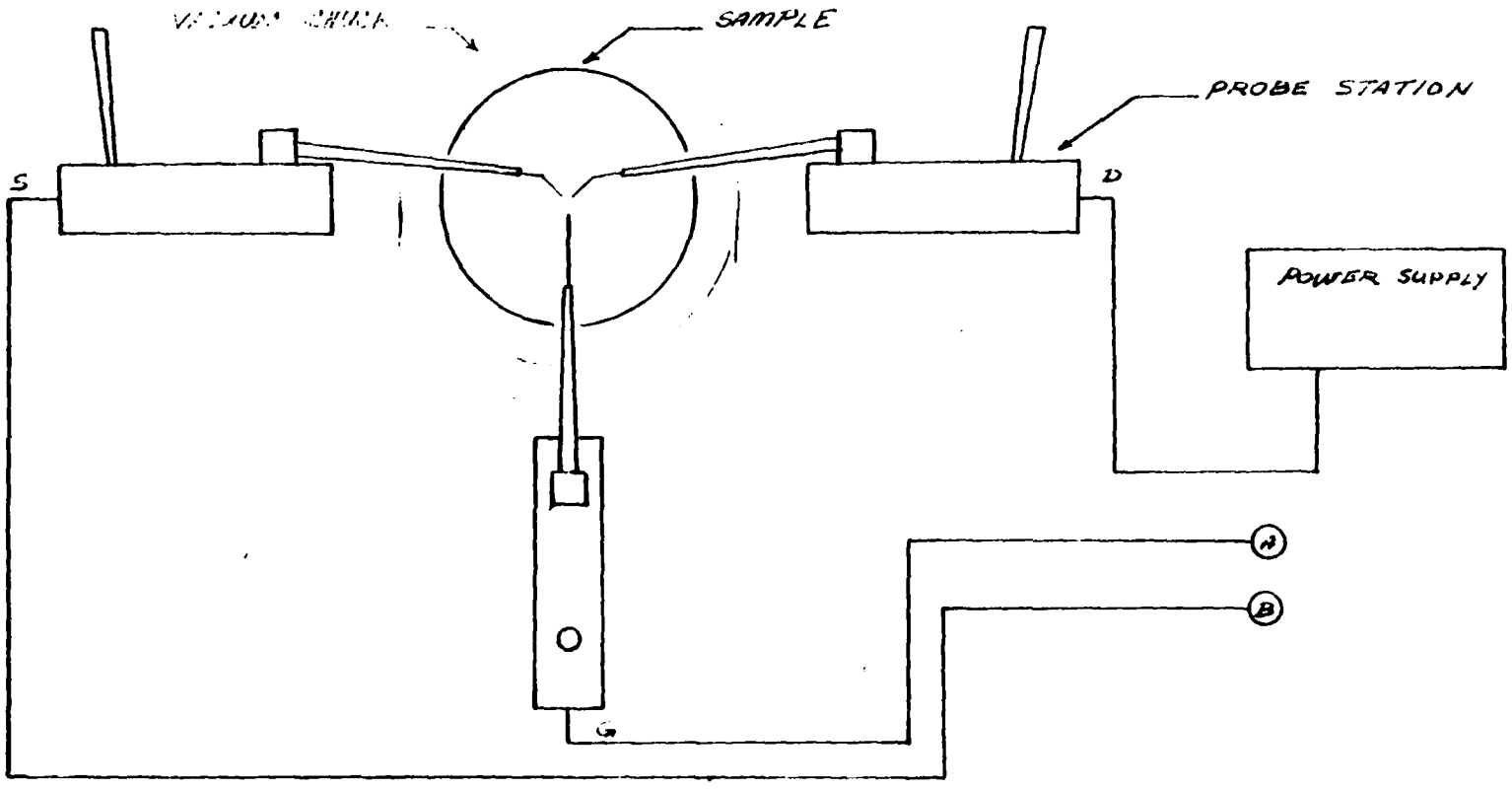
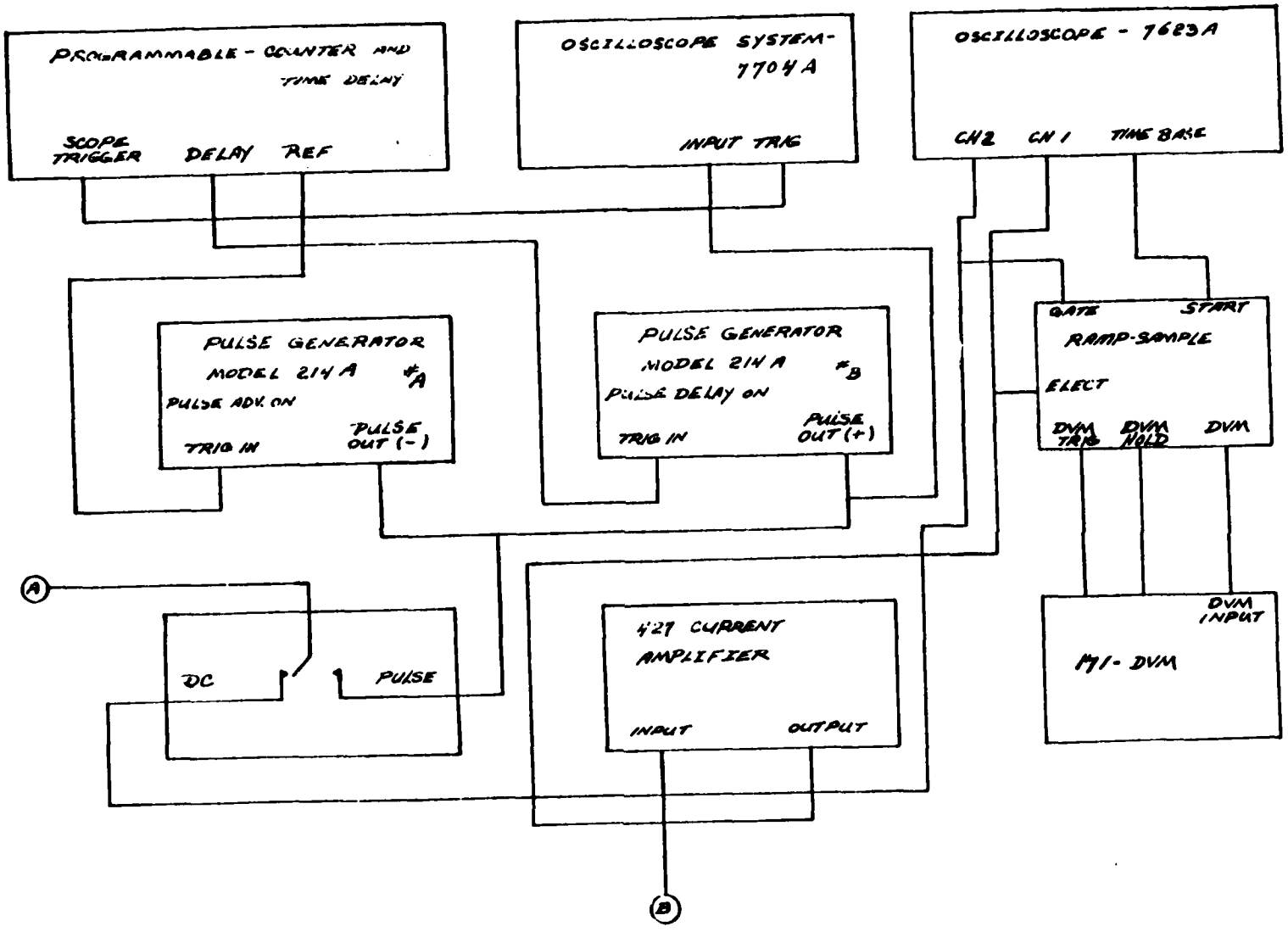
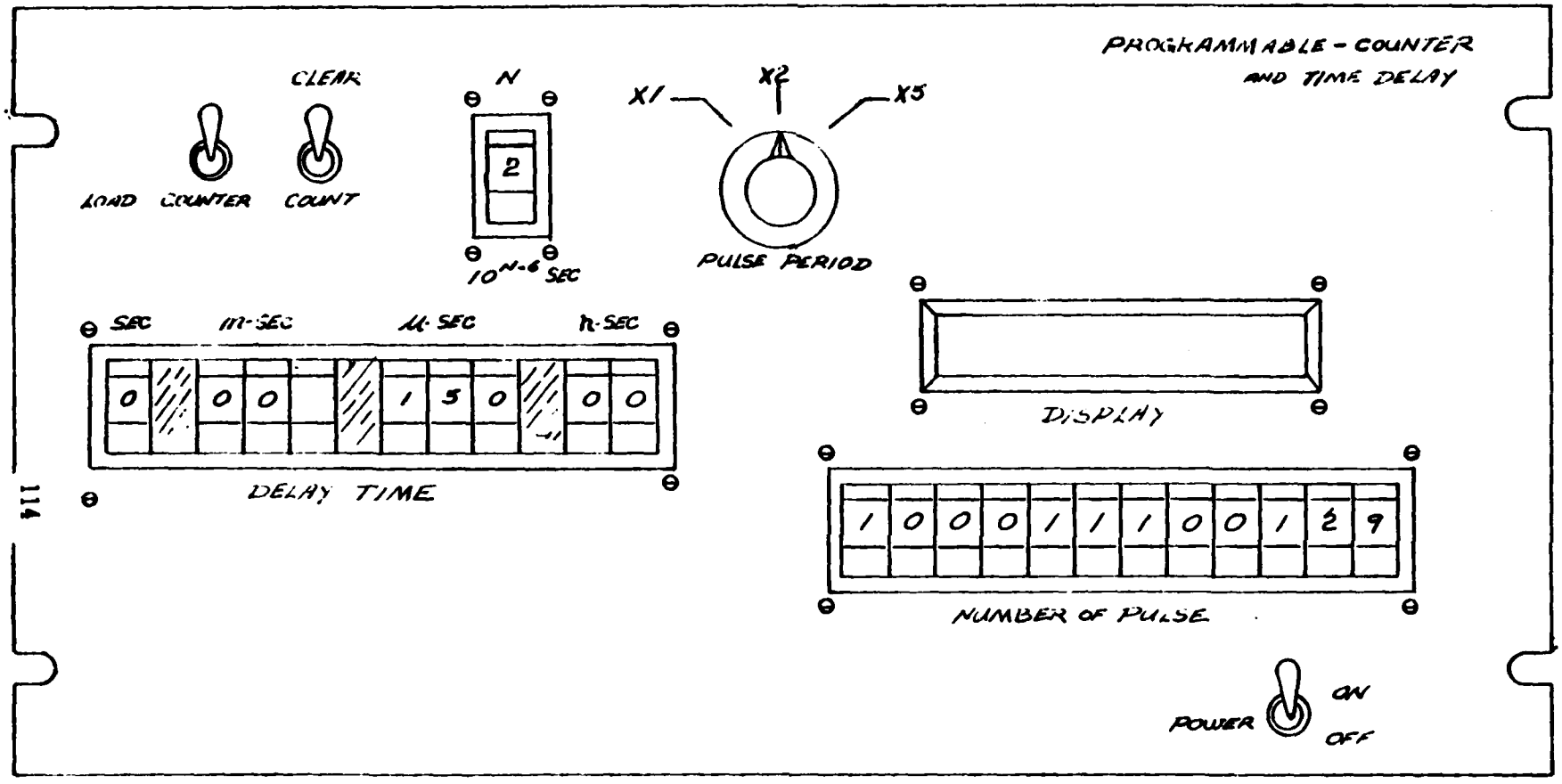


Figure 1



SYSTEM BLOCK DIAGRAM

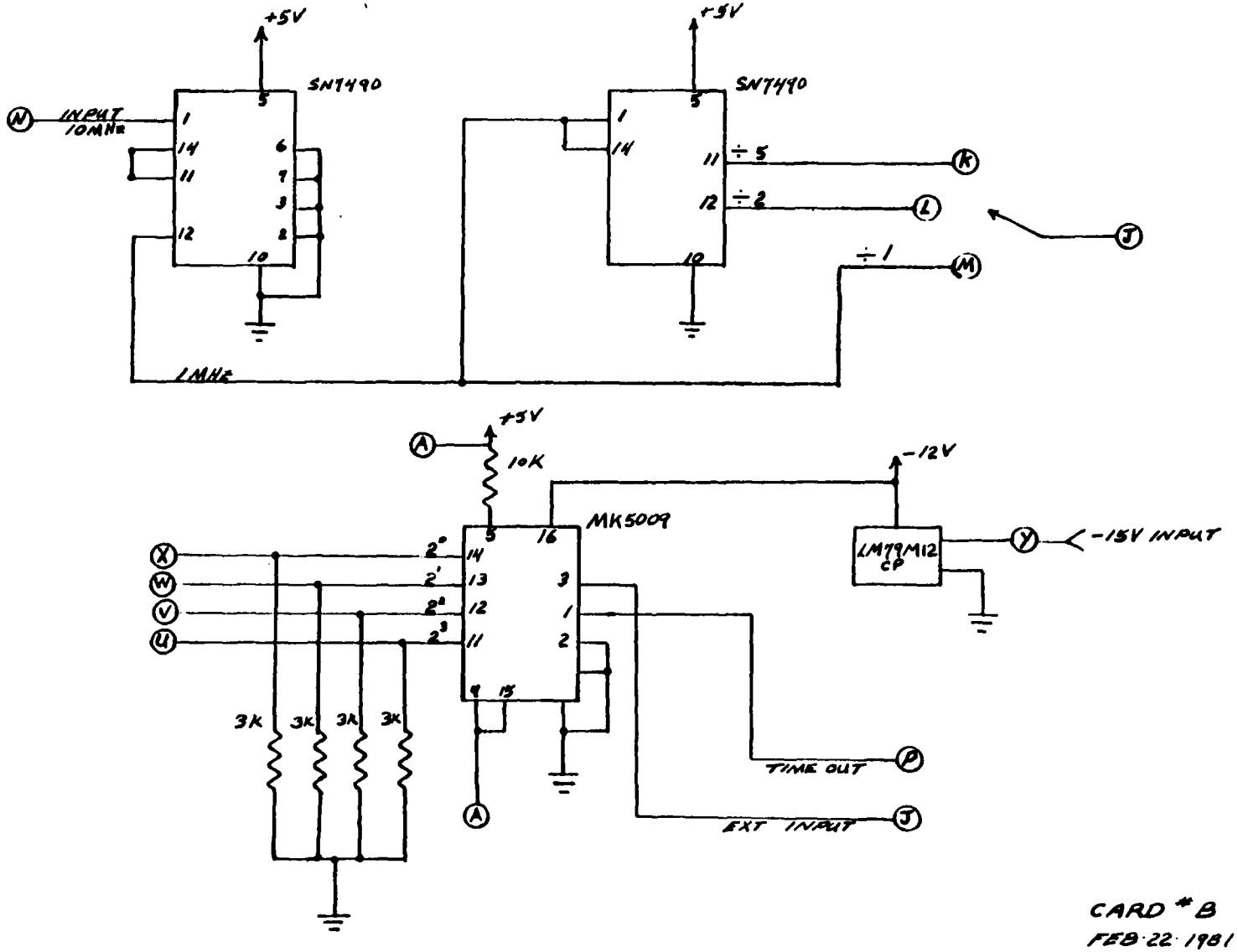
Figure 2



CONTROL PANEL LAYOUT

Figure 3

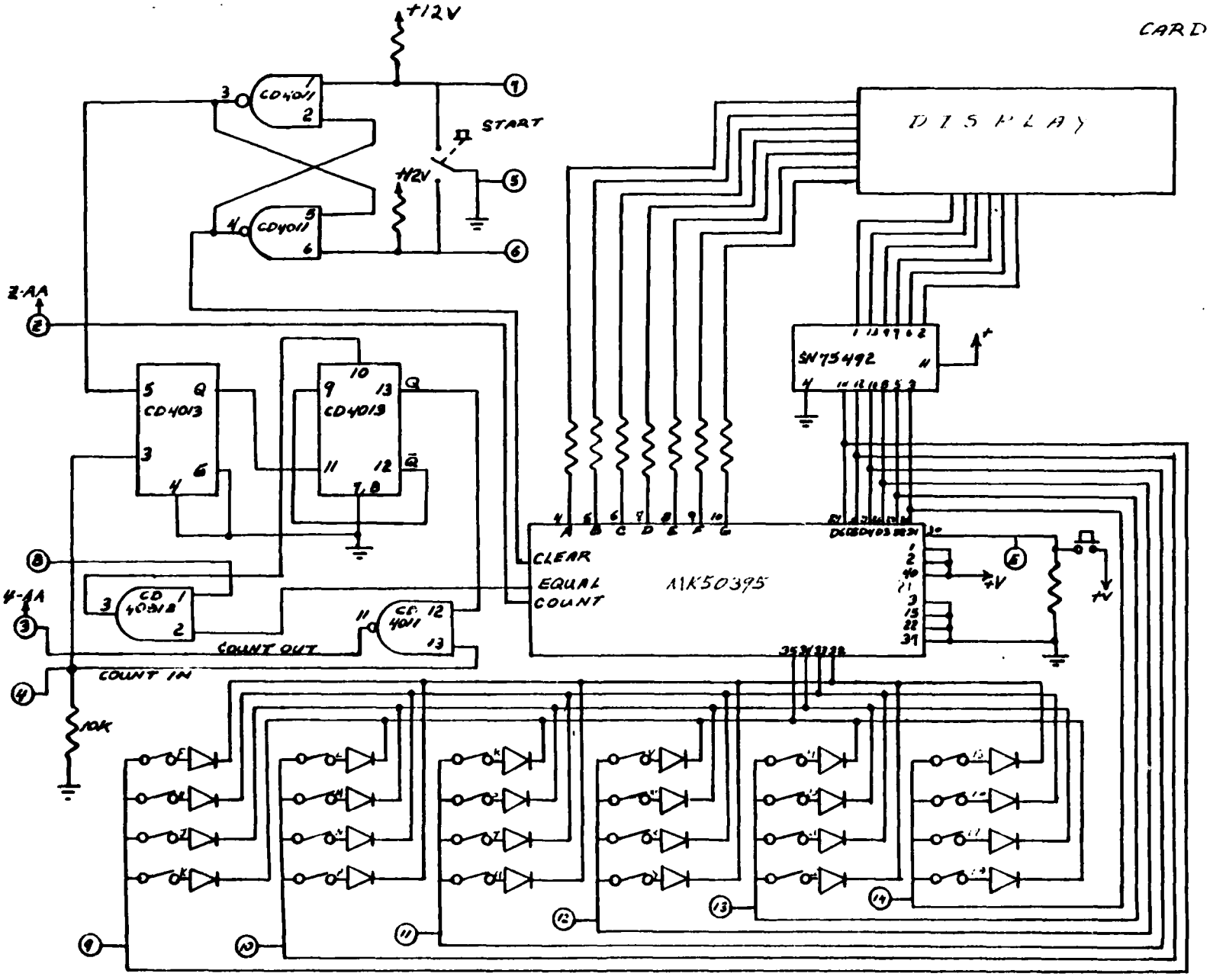
Appendix - A



CARD # B
FEB 22 1981

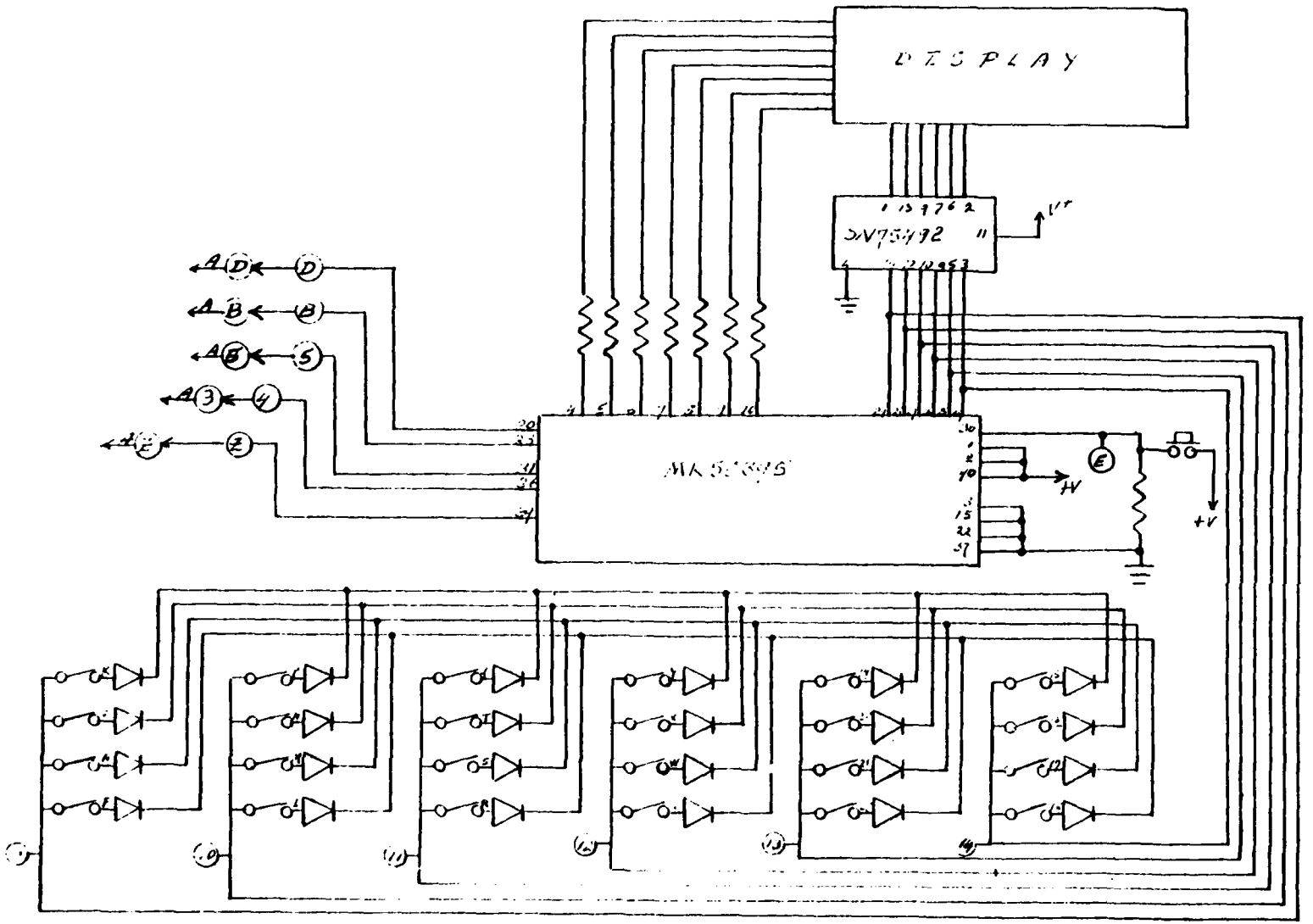
TIME BASE CIRCUIT

Figure A-1



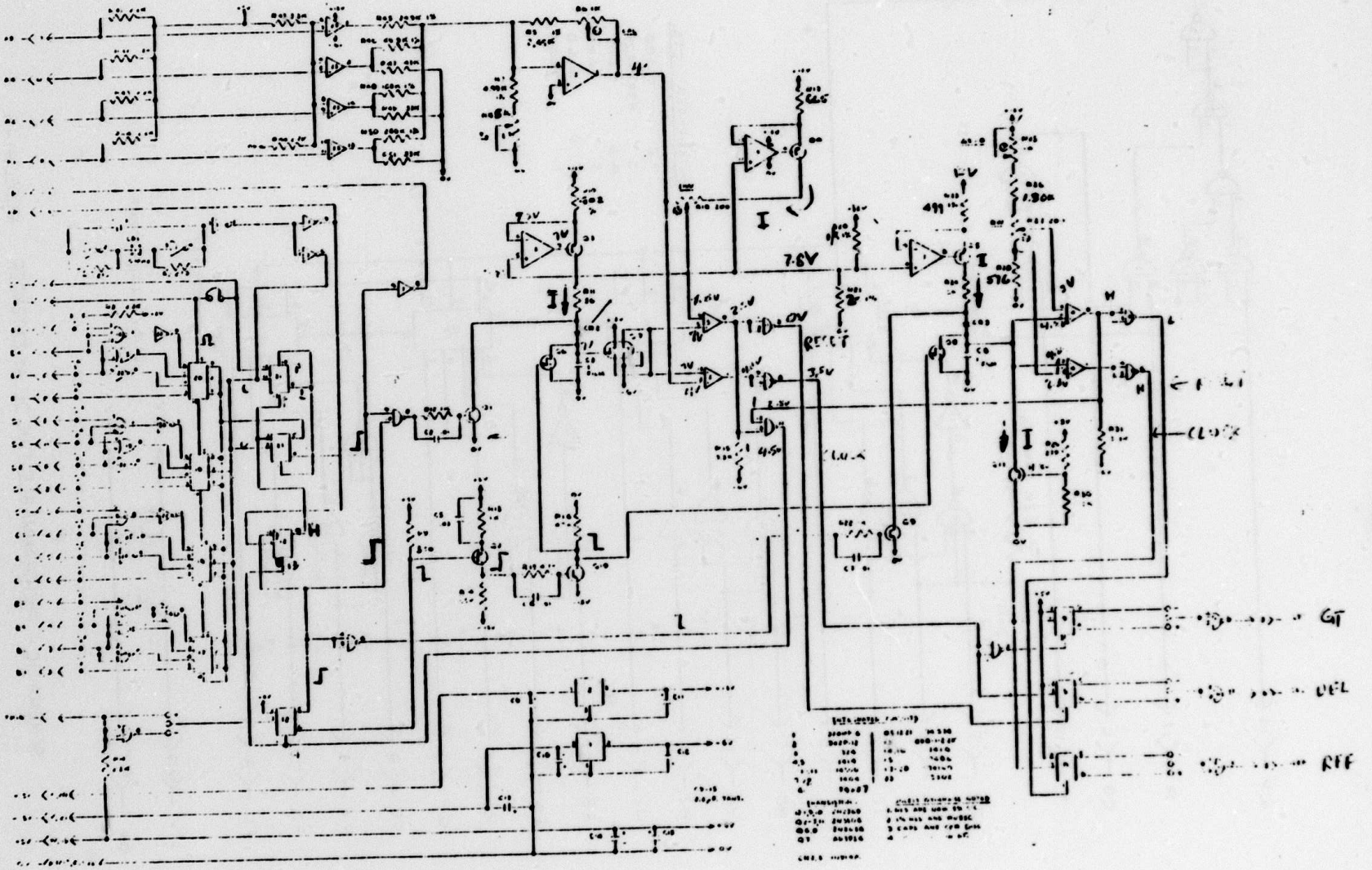
COUNTER CIRCUIT

Figure A-2



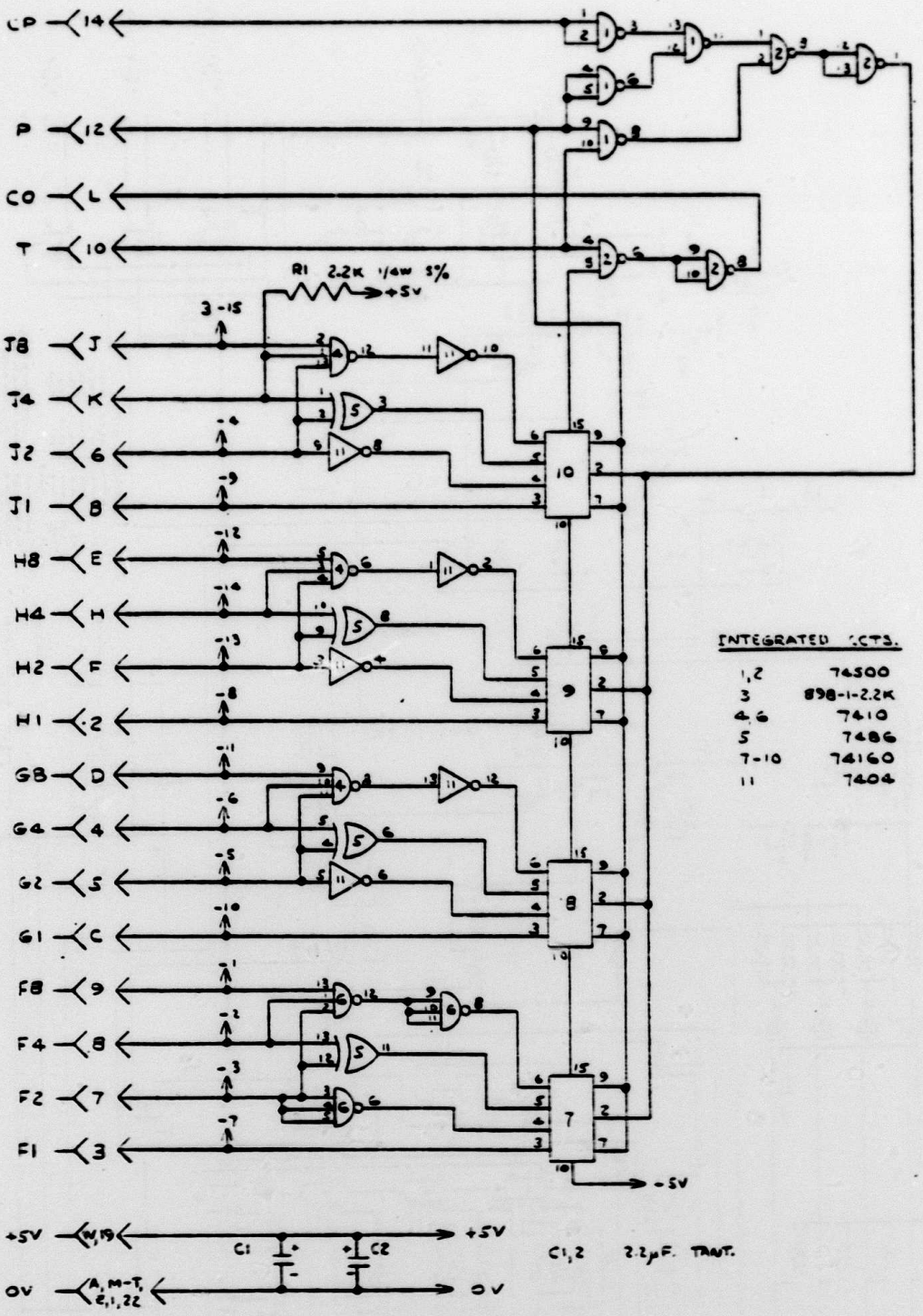
COUNTER CIRCUIT

Figure A-3



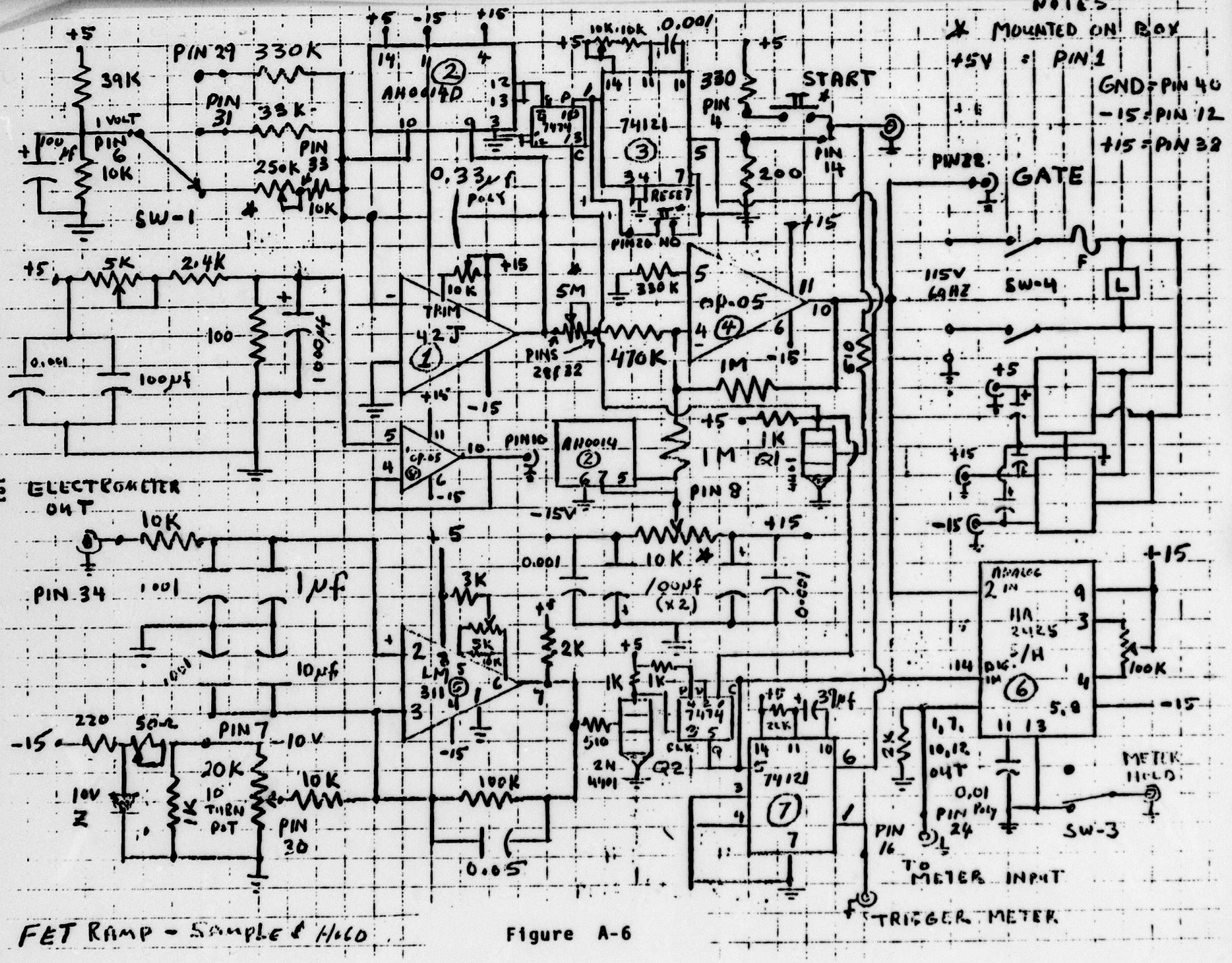
SCHEMATIC PROGRAMMABLE TIME DELAY MODEL 4145-2

Figure A-4



SCHEMATIC – PROGRAMMABLE TIME DELAY EXTENDER MODEL 4146

Figure A-5



FET Ramp - Sample & Hold

Figure A-6